Compared to the PT-IGBT, the NPT-IGBT shows the following advantages resulting from diminished emitter efficiency, longer charge carrier life time and more exact design possibilities, which is still to be detailed in chapters 2 and 3:

- positive on-state voltage temperature coefficient (”automatic” static balancing in the case of parallel connection),
- lower, but partly longer turn-off tail current; lower turn-off losses at $T_j$ = 125°C,
- (in the case of hard switching) shorter switching times and reduced switching losses,
- considerably reduced temperature dependency of switching times / switching losses ($T_j$ = 125°C) and tail current,
- increased overcurrent stability by improved current limitation in case of overload.

Compared to the epitaxial substrates of the PT-IGBT, today’s production of the homogeneous $n^-$-substrate as basic material for NPT-IGBTs is more favourable, provided that the much thinner silicon wafers are handled properly.

### 1.2.2 Static behaviour

In this chapter the static behaviour of power MOSFETs- and IGBT-modules is to be examined regarding the current-voltage characteristics of the main terminals in the $I^{st}$ and $III^{rd}$ quadrant of the respective output characteristic (Figure 1.7).

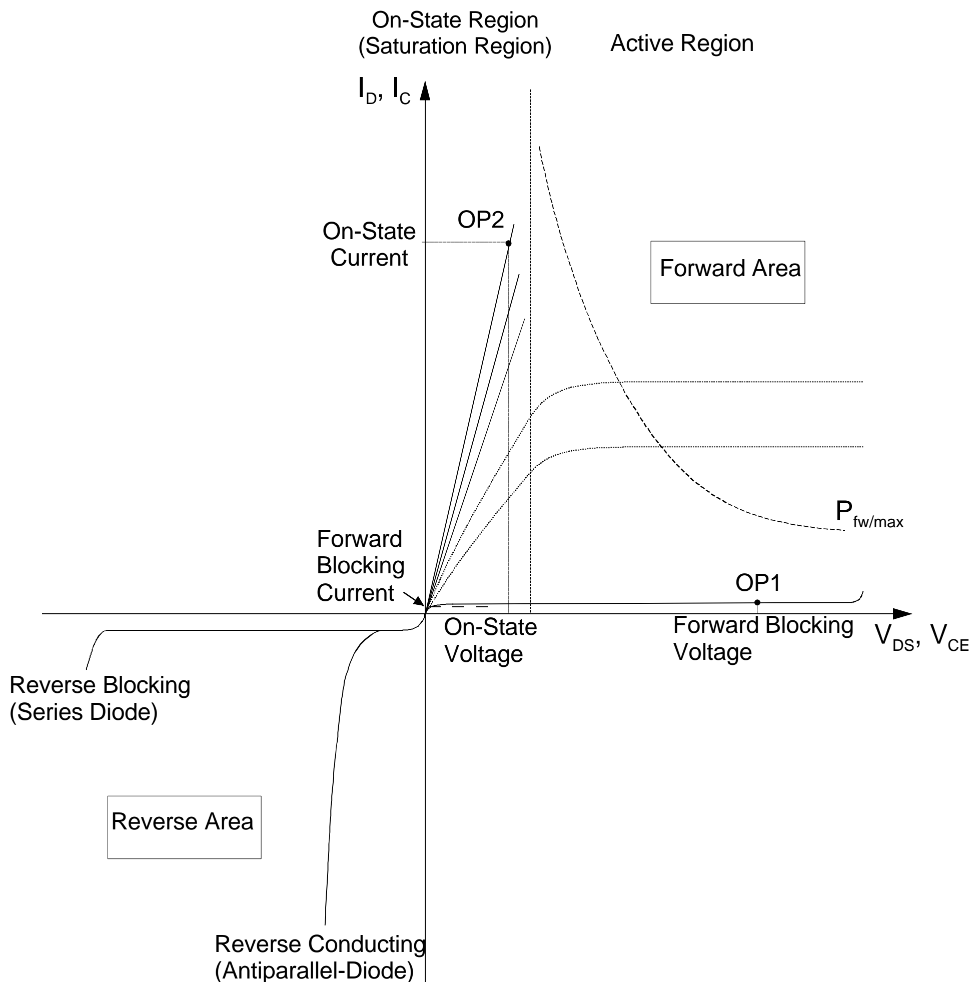


Figure 1.7 Basic output characteristic of a power transistor module

The $I^{st}$ quadrant shows the *forward area*, where power transistor modules can block high voltages and switch high currents.

The exact designation "*blocking state*" - analogous to thyristors - for blocking in the $I^{st}$ quadrant is hardly used in connection with transistors. Usually, this is called „*forward off- state*" (as in the following explanations) or „*off-state*" (as long as there is no risk of confusion).

Via the gate electrode, the power-MOSFET or IGBT is turned from the *forward off- state* (OP1 in Figure 1.7) to the *conductive state* or *on-state* (OP2), where it can conduct load current. The *active* region is only passed during switching.
Contrary to the „perfect switch" off-state voltage and on-state current are limited (see chapter 0).
During the forward off-state a cut-off current (*forward off-state current*) causes blocking power dissipation within the transistors.

In the conductive state the voltage left at the main power terminals depends on the on-state current and is called *on-state voltage*, causing on-state power dissipation. The maximum power dissipation during on-state (not during switching) is shown by the on-state power dissipation hyperbola for $P_{fw/max}$ in the output charcteristic.

The current-voltage characteristics in the $III^{rd}$ quadrant of the output characteristic show the *reverse* behaviour of power transistor modules, in case a negative voltage is applied to the main terminals. This behaviour is determined by the characteristics of the transistors (reverse blocking, reverse conducting) and the features of the diodes within the power module (connected in series or anti-parallel to the transistors).

#### *1.2.2.1 Power-MOSFET*

The functional principles of the power-MOSFET described above result in the output characteristics in Figure 1.8a.

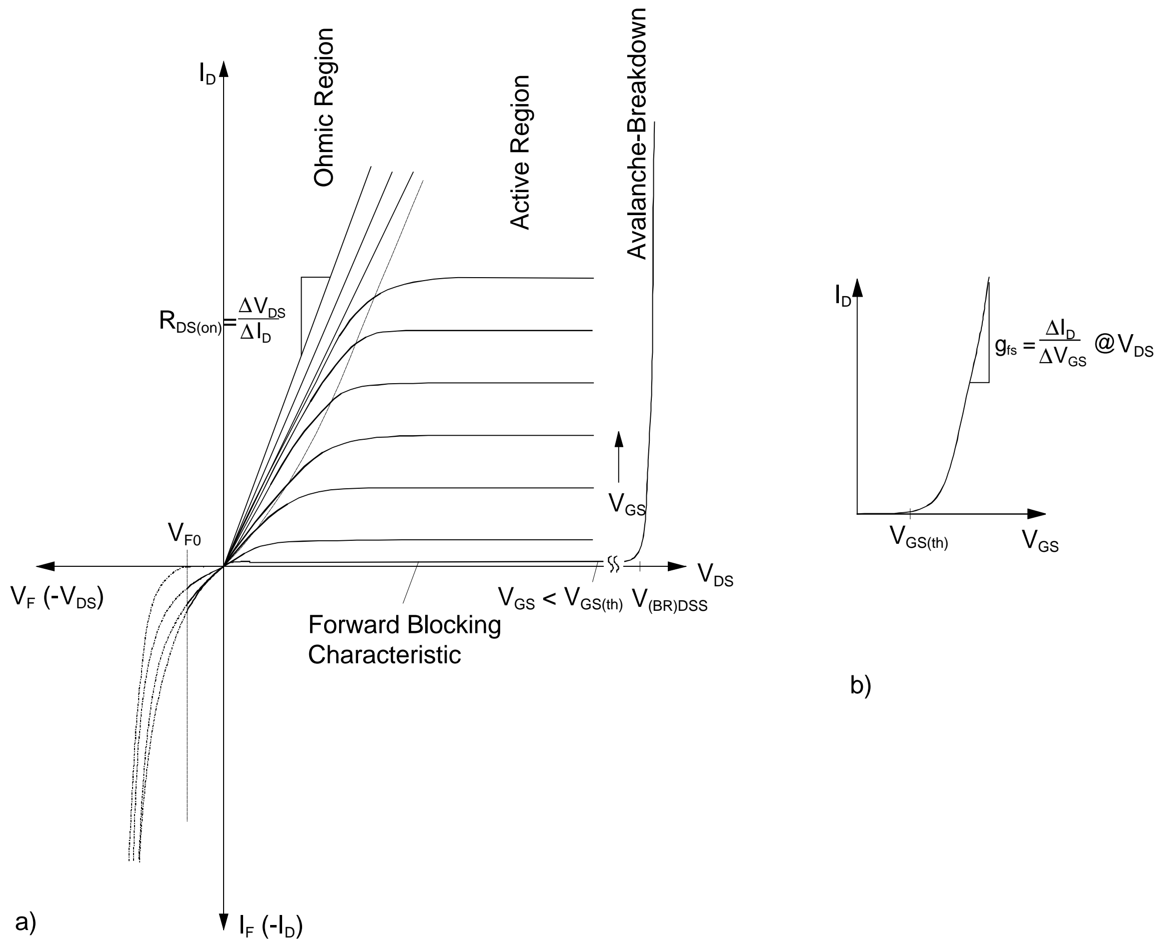


Figure 1.8 a) Output characteristics of a power-MOSFET (n-channel-enhancement-type)
b) Transfer characteristic $I_D = f(V_{GS})$

*Forward off-state*

When applying a positive drain-source voltage $V_{DS}$ and a gate-source voltage $V_{GS}$ smaller than the gate-source threshold-voltage $V_{GS(th)}$, there will only be a very small zero gate voltage drain current $I_{DSS}$ between drain- and source connection.

$I_{DSS}$ will rise slightly with increasing $V_{DS}$. If a certain specified maximum drain-source voltage $V_{DSS}$ is exceeded, this will cause an avalanche breakdown of the pin-junction $p^+$-well/$n^-$-drift zone/$n^+$-epitaxial layer (breakdown voltage $V_{(BR)DSS}$). Physically, $V_{(BR)DSS}$ is almost equivalent to the breakdown voltage $V_{CER}$ of the parasitic bipolar npn-transistor in a MOSFET, generated by the sequence of layers: $n^+$-source zone (emitter)/$p^+$-well (base)/$n^-$-drift zone/$n^+$-epitaxial layer-drain connection (collector), see Figure 1.3.
The multiplication current generated by the avalanche breakdown of the collector-base diode may lead to destruction of the MOSFET as soon as the bipolar transistor is turned on.
However, the base and emitter zones are almost short-circuited by metallization of the source; both zones are only separated by the lateral resistance of the $p^+$-well.
Several structural improvements, such as small MOSFET cells, homogeneous cell arrangement, low-resistive p+-wells, optimized marginal structures and highly homogeneous technological procedures, may facilitate a very small avalanche breakdown current per cell in modern MOSFETs, so that the bipolar transistor will not yet be turned on, in case the defined specifications are strictly complied with.

Therefore, a permissible avalanche energy $E_A$ for single pulses or periodic load (limited by the maximum chip temperature) can be defined; see chapter 2.2.1.
Since several parallelled MOSFET-chips in power modules cannot guarantee absolute symmetrical conditions, the maximum $E_A$-value is only applicable for one single chip.

*On-state*

The forward on-state at positive drain-source voltage $V_{DS}$ and positive drain current $I_D$ can be divided into two characteristic regions (Figure 1.8, $I^{st}$ quadrant).

**Pinch-off or active region**

At a gate-source voltage $V_{GS}$ slightly exceeding the threshold voltage $V_{GS(th)}$, current saturation will cause a considerable drop of voltage over the channel (horizontal region of the output characteristic). The drain current $I_D$ is controlled by $V_{GS}$.
The transfer behaviour shown in Figure 1.8b is called *forward transconductance* $g_{fs}$ defined as follows:

$g_{fs} = dI_D/dV_{GS} = I_D/( V_{GS}-V_{GS(th)})$.

Forward transconductance in the pinch-off region rises proportionally to the drain current $I_D$ and the drain-source-voltage $V_{DS}$ and drops with increasing chip temperatures.
Within the permissible operation conditions for power modules with several paralleled MOSFET-chips, the pinch-off region is only passed during turn-on and turn-off.
On the other hand, stationary operation within the pinch-off region is mostly prohibited by the manufacturer, because $V_{GS(th)}$ will drop when the temperature rises and, therefore, thermal instability between the single chips might result from minor production deviations.

**Ohmic region**

The ohmic region, which is also called on-state during switching operations, is reached as soon as $I_D$ is determined only by the outer circuit. The on-state behaviour can be characterized as the quotient of changed drain-source-voltage $V_{DS}$ and drain-current $I_D$ via the turn-on resistance $R_{DS(on)}$. Consequently, the forward voltage $V_{DS(on)}$ may be defined by the following equation already mentioned in chapter 1.2.1 (large-signal behaviour)

$$V_{DS(on)} = R_{DS(on)} \cdot I_D$$

$R_{DS(on)}$ is dependent on the gate-source voltage $V_{GS}$ and the chip temperature. $R_{DS(on)}$ is approximately doubled within the MOSFET operation temperature range between 25°C and

*Reverse operation*

During reverse operation ($III^{rd}$ quadrant) the MOSFETcharacteristic is equivalent to a diode characteristic at $V_{GS} < V_{GS(th)}$ (continuous curve in Figure 1.8a). This is caused by the parasitic diode within the MOSFET; the MOSFET reverse on-state behaviour at closed channel is controlled by the on-state voltage of the collector-base pn-junction or source-drain pn-junction, respectively („inverse diode“, *bipolar current flow*) (Figure 1.9a).

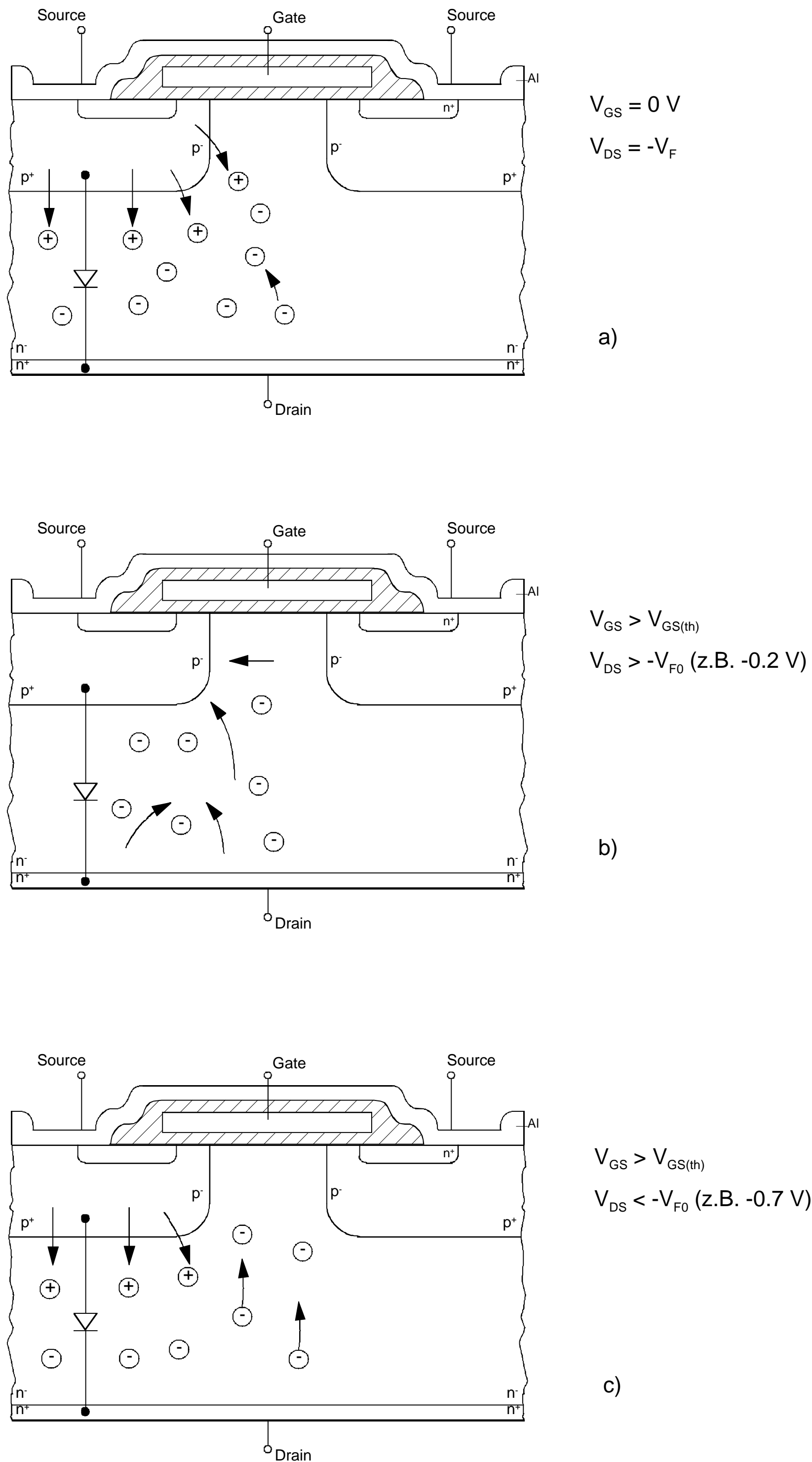


Figure 1.9 Inverse operation of a power-MOSFET [277]
a) At closed channel (bipolar current flow)
b) At open channel and small negative $V_{DS}$ (unipolar current flow)
c) At open channel and big negative $V_{DS}$ (combined current flow)

The bipolar inverse diode is utilized for currents up to the limit values specified for MOSFETs. In practice, however, the inverse diode

- causes relatively high on-state power losses, which have to be dissipated together with the MOSFET power losses and

- sets limits to the MOSFET's application field as a „hard switch“ (see chapter 0) by its unfavourable turn-off behaviour.

As shown in Figure 1.9b the conductance in the MOSFET-channel is principally controllable even at a negative drain-source-voltage, if a gate-source voltage is applied exceeding the threshold voltage.
If the drain-source voltage is limited to a value lower than the inverse diode threshold voltage by external components, for example by paralleling of a Schottky-diode, the inverse current will be conducted from drain to source as a *unipolar electron current* (majority carrier current). Then, the turning-off corresponds to the turn-off behaviour of a MOSFET.
The inverse current is dependent on $V_{DS}$ and $V_{GS}$. (broken curve in Figure 1.8a).

Operation with *combined current flow* according to Figure 1.9c (semi-coloned curve in Figure 1.8a) is given, if the channel is open and a conducting bipolar inverse diode is connected (drain-source voltage higher than diode threshold voltage). This results in a reduced on-state voltage compared to simple paralleling of diode and MOSFET, since the injected charge carriers will also diffuse laterally, thus increasing the MOSFET's conductivity.

Apart from that, MOSFET-chips with fast inverse diodes have been developed by several manufacturers during the past few years (e.g. FREDFETs; **F**ast **R**ecovery **E**pitaxial **D**iode **F**ield **E**ffect **T**ransistors)[277]. Hole life time at inverse operation is minimized in FREDFET-chips by selective heavy-metal diffusion into the $n^-$-drift area, similar to the design of fast diodes.

### *1.2.2.2 IGBT*

The functional principle of the IGBT described in chapter 1.2.1 results in the output characteristic in Figure 1.10.

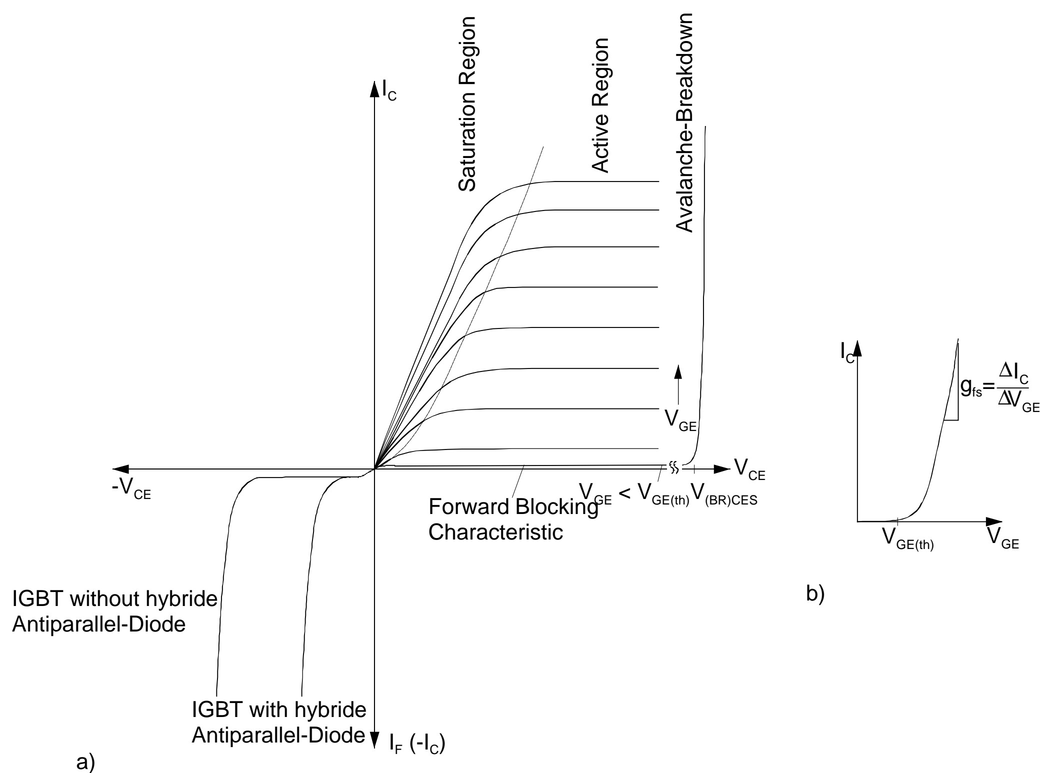


Figure 1.10 a) Output characteristic of an IGBT (n-channel-enhancement-type)
b) Transfer characteristic $I_C = f(V_{GE})$

*Forward off-state*

In analogy to the MOSFET, the collector-emitter cut-off current $I_{CES}$ between collector and emitter is only very small, if the collector-emitter voltage $V_{CE}$ is positive and the gate-emitter voltage $V_{GE}$ is lower than the gate-emitter threshold voltage $V_{GE(th)}$ .
As a consequence of increasing $V_{CE}$, the $I_{CES}$-value rises slightly. When a certain specified maximum collector-emitter voltage $V_{CES}$ is exceeded, there will follow an avalanche breakdown of the pin-junction layers $p^+$-well/$n^-$-drift zone/$n^+$-epitaxial layer (avalanche breakdown voltage $V_{(BR)CES}$). Physically, $V_{(BR)CES}$ corresponds approximately to the reverse collector-emitter voltage $V_{CER}$ of the *bipolar pnp-transistor* in the IGBT structure. (see Figure 1.6).
The multiplication current generated by the avalanche breakdown of the collector-base diode may lead to destruction of the IGBT, as soon as the bipolar transistor is turned on.
However, base and emitter are almost short-circuited by metallization of the emitter, only separated by the lateral resistance of the $p^+$-well.
By several structural improvements within the IGBT, similar to the measures taken for MOSFETs as described in chapter 1.2.2.1, the avalanche breakdown current per cell is kept at a minimum level, which results in a high forward off-state voltage stability (avalanche stability).

*On-state*

Also with the IGBT, the forward on-state at a positive collector-emitter voltage $V_{CE}$ and a positive collector current $I_C$ can subdivided up in two characteristic regions (Figure 1.10, I$^{st}$ quadrant).

**Active region**

At a gate-emitter voltage $V_{GE}$ slightly exceeding the threshold voltage $V_{GE(th)}$, current saturation will cause a considerable voltage drop over the channel (horizontal region of the output characteristics). The collector current $I_C$ is controlled by $V_{GE}$.
The transfer behaviour shown in Figure 1.10b is called - in analogy to the MOSFET - *forward transconductance* $g_{fs}$ defined as follows:

$$g_{fs} = dI_C/dV_{GE} = I_C/(V_{GE}-V_{GE(th)})$$

Forward transconductance in the cut-off region rises proportionally to the collector current $I_C$ and the collector-emitter voltage $V_{CE}$, and decreases with increasing chip temperatures.
Within the permissible operation conditions for power modules with several paralleled IGBT-chips, the cut-off region is only passed during turn-on and turn-off.
Equivalent to MOSFET modules, stationary operation within the cut-off region will mostly be prohibited, since $V_{GE(th)}$ will decrease when the temperature rises and, also with IGBTs, thermal instability between the single chips might result from minor production deviations.

**Saturation region**

The saturation region (steep region of the output characteristic), also called on-state during switching operation, is reached as soon as $I_C$ is determined only by the outer circuit. The on-state behaviour is characterized by the IGBT voltage $V_{CEsat}$ (collector-emitter saturation voltage). At least for highly blocking IGBTs, the saturation voltage is considerably smaller than the on-state voltage of a comparable MOSFET due to the $n^-$-drift-zone being flooded with minority carriers.
As already mentioned, $V_{CEsat}$ of PT-IGBTs will drop at a temperature increase within rated current operation, whereas $V_{CEsat}$ of NPT-IGBTs will rise proportionally to the temperature.