

### Reverse operation

During reverse operation (Figure 1.10, III<sup>rd</sup> quadrant) the IGBT collector pn-junction is poled in reverse direction and there is no inverse conductivity, other than with MOSFETs.

Although, due to the large n<sup>-</sup>-drift zone, this is actually the structure of a highly resistive pin-diode, at least in the case of NPT-IGBTs, the reverse voltage in today's IGBTs is only some 10V. Apart from design of the chip margin, this is due to the fact that the chips have been designed mainly to comply with a high off-state voltage and an optimized collector heat dissipation.

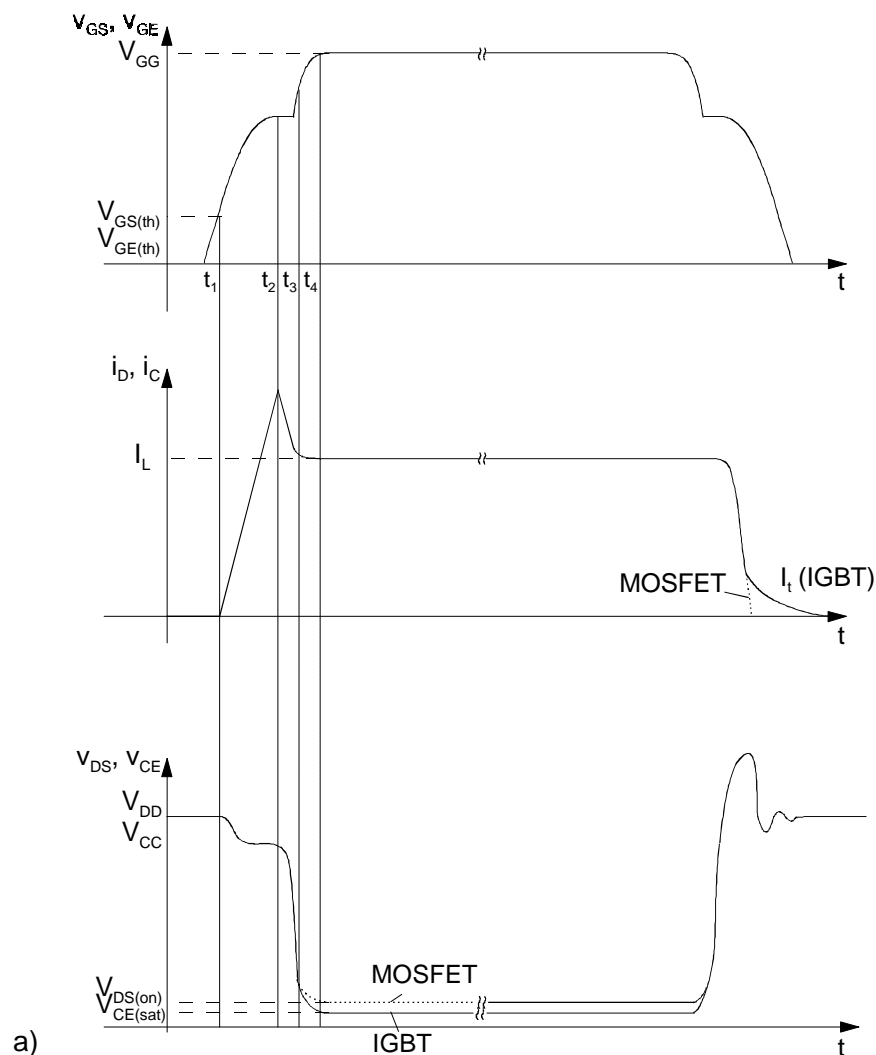
IGBT-switches designed for special reverse applications have therefore been equipped solely with adapted, fast hybrid diodes connected in series.

So, the characteristics of the external or hybrid diodes (see chapter 1.3) are exclusively responsible for the reverse on-state behaviour of IGBT-modules.

### 1.2.3 Hard switching behaviour of MOSFETs and IGBTs

Most switching applications for transistor switches require „hard“ switching of ohmic-inductive loads with continuous load current, i.e. the time constant of the load  $L/R$  is much bigger than the cycle  $1/f$  of the switching frequency.

The resulting basic waveforms for drain or collector current and drain-source or collector-emitter voltage are shown in Figure 1.11a.



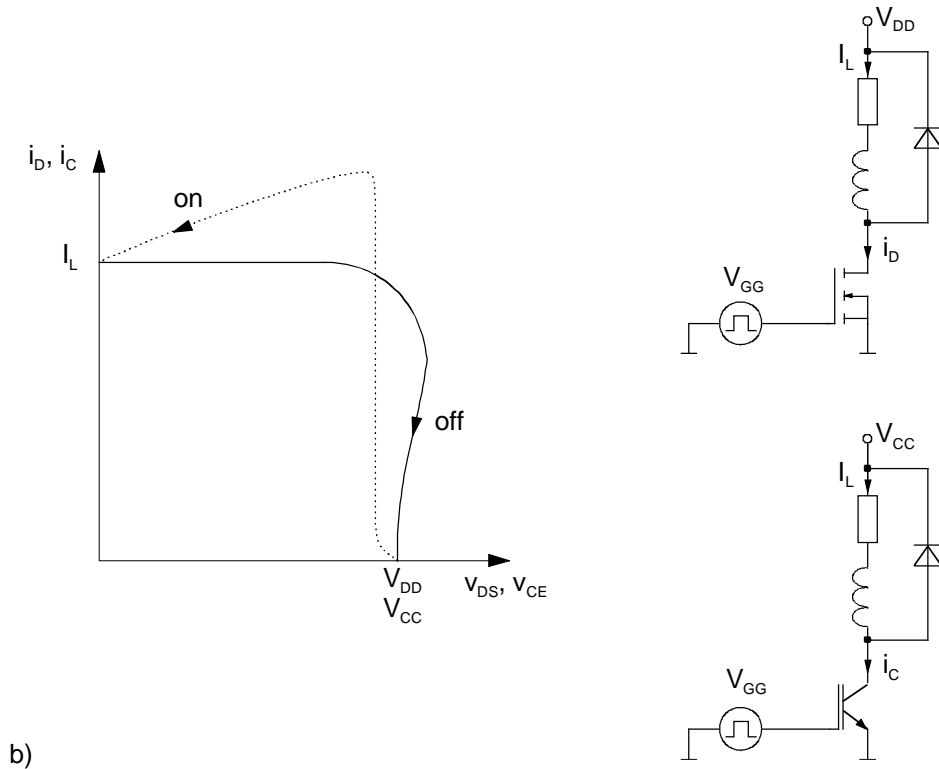


Figure 1.11 Typical “hard” switching behaviour of MOSFET and IGBT (ohmic-inductive load with free-wheeling circuit)  
 a) Current and voltage waveforms  
 b) Curve and measurement circuit

As already depicted in chapter 0, Figure 0.4 a high short-time transistor current and voltage during turn-on and turn-off are typical features of „hard switching“.

In contrast to all types of thyristors, such transistors operate without passive snubber networks thanks to the „dynamic“ junction which is generated in the drift zone during switching operation. In a transistor, however, considerable switching energy

$$E_{on}, E_{off} = \int_{t_{on}, t_{off}} u \cdot idt$$

is dissipated as explained by the graph  $i_C = f(v_{CE})$  (and  $i_D = f(v_{DS})$ ) in Figure 1.11b.

The curve may be directed nearer towards the axes with passive snubber networks. Switching losses are „shifted“ from the transistor to the snubber, the total efficiency will decrease in most cases (chapter 3.8).

Since the size of the operating area is influenced by many (non-ideal) transistor features apart from current/ voltage limitations and switching times, the SOA (**S**afe **O**perating **A**rea) is given in the datasheets for different operating conditions (see chapters 2.1.2, 2.2.3 and 2.3.3).

Moreover, passive circuit elements have a tremendous influence on switching losses and operating areas, apart from the non-ideal transistor features and the diode characteristics described in chapter 1.3. The effects of such passive circuit elements also indicated in Figure 1.11a are explained in detail in chapter 3.4.1.

Physically, the typical current-voltage characteristics in Figure 1.11a are caused by the free-wheeling diode, which has to prevent current snap-off by load inductance:

- When the transistor is turned on, the free-wheeling diode can only take up reverse recovery voltage (turn off), after the load current has completely commutated to the transistor. Therefore, the collector or drain-current has to reach the load current level, before the collector-emitter (or drain-source) voltage may fall to the on-state value.
- When the transistor is turned off, the free-wheeling diode can only take up the load current (turn on), after it has reached on-state voltage polarity. This will be the case when the collector-emitter (or drain-source) voltage has exceeded the commutation voltage level, before the collector or drain-current may fall to the cut-off current value.

As shown in Figure 1.11a, the drain-source or collector-emitter voltage of comparable components will, shortly after *turn-on* of the MOSFET or IGBT, drop within some 10ns to a value, that is equivalent to the voltage drop over the  $n^-$ -drift area. Whereas in the MOSFET the on-state voltage has already been reached by this, the  $n^-$ -area of the IGBT is now flooded with positive charge carriers from the p-collector zone. After this procedure has been finished (appr. 100ns up to some  $\mu$ s), the static value of the on-state saturation voltage  $V_{CE(sat)}$ , which is relatively low for highly blocking components, has been reached (conductivity modulation).

During *turn-off* of the MOSFET, the internal capacitances have to be recharged, that there are no charge carrier influence left in the channel area. Thereafter, the neutrality interferences in this area will quickly be reduced and the drain current will drop rapidly.

The procedure within the IGBT is principally the same. However, after the emitter current in the  $n^-$ -drift zone has been turned off, a large number of p-charge carriers generated by injection from the IGBT-collector zone is still left. These p-charge carriers have now to be recombined or reduced by re-injection, which would cause a so-called collector tail current  $I_t$ . (Figure 1.11a).

Since this tail current will fade away within some  $\mu$ s only with already increased collector-emitter voltage, the hard turn-off power losses in the IGBT are mainly determined by the tail current waveform (see chapter 2.3.2, 3.1.3) and are considerably higher than those in MOSFETs.

Apart from the explained differences, the switching behaviour of MOSFETs is very similar to that of IGBTs due to the equivalent gate structure.

As described in chapter 1.2.1, the forward on-state and forward off-state capability, the reverse behaviour and the limits of the transient currents and voltages during switching are influenced by the *internal structures of the bipolar transistor* and the *lateral resistances*.

The switching behaviour (switching velocity, switching losses) of MOSFET and IGBT power modules is determined by their structural, *internal capacitances (charges)* and the *internal and outer resistances*.

Contrary to the ideal of a powerless voltage control via the MOSFET or IGBT gate, a frequency-dependent *control power* is required resulting from the necessary *recharge currents* of the internal capacitances, see chapter 3.5.

Moreover, the commutation processes are affected by the *parasitic connection inductances* existing in the power layout and generated by connection of transistor chips in power modules; they induce transient overvoltages and may cause oscillations due to the circuit and transistor capacitances (see chapter 3.4).

In the following, the switching behaviour of MOSFETs and IGBTs is to be analysed in relation to the internal capacitances and resistances of the transistor.

When the MOSFET (IGBT) is turned off,  $C_{GD}$  ( $C_{GC}$ ) is low and is approximately equal to  $C_{DS}$  ( $C_{CE}$ ).

During on-state  $C_{GD}$  ( $C_{GC}$ ) will increase rapidly due to inversion in the enhancement layer below the gate zones, as soon as the gate-source (emitter) voltage has exceeded the drain-source (collector-emitter) voltage.

Additionally,  $C_{GD}$  ( $C_{GC}$ ) will increase dynamically during the switching procedure due to the Millereffect:

$$C_{GDdyn} = C_{GD} (1 - dv_{DS}/dv_{GS}) \text{ (MOSFET)}$$

$$C_{GCdyn} = C_{GE} (1 - dv_{CE}/dv_{GE}) \text{ (IGBT)}$$

In most datasheets the following voltage-dependent low-signal capacitances of turned off transistors are given (see chapters 2.2.2, 2.2.3).

Power MOSFET	IGBT	
$C_{iss} = C_{GS} + C_{GD}$	$C_{iss} = C_{GE} + C_{GC}$	Input capacitance
$C_{rss} = C_{GD}$	$C_{rss} = C_{GC}$	Reverse transfer capacitance
$C_{oss} = C_{GD} + C_{DS}$	$C_{oss} = C_{GC} + C_{CE}$	Output capacitance

For calculation of the switching behaviour, these datas may only be applied to a certain extent, since e.g.  $C_{iss}$  and  $C_{rss}$  will again increase enormously in a fully switched on transistor ( $V_{DS} < V_{GS}$  bzw.  $V_{CE} < V_{GE}$ ), a fact that is not considered in most datasheets (Figure 1.12 and Figure 1.13) [277].

Therefore, switching times in relation to gate current, drain-source voltage and drain current are determined with the aid of the MOSFET “gate charge characteristic” indicated in the datasheets, plotting the gate-source voltage over the gate charge  $Q_G$  on condition of “rated current” and 20 % or 80 % of the maximum drain-source voltage (Figure 1.12).

Load conditions and measurement circuit are equivalent to Figure 1.11. However, for simplification purposes, constant current is supposed to be fed to the gate.

Now, switching intervals may be determined very simply with the following relation (see chapter 3.5.1):

$$i_G = dQ_G/dt$$

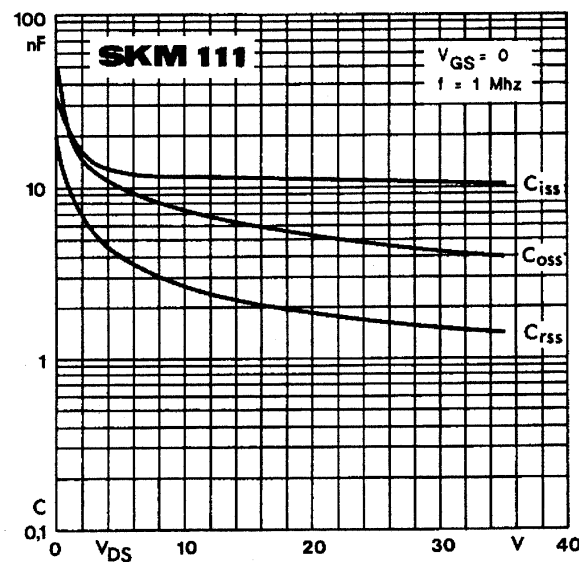
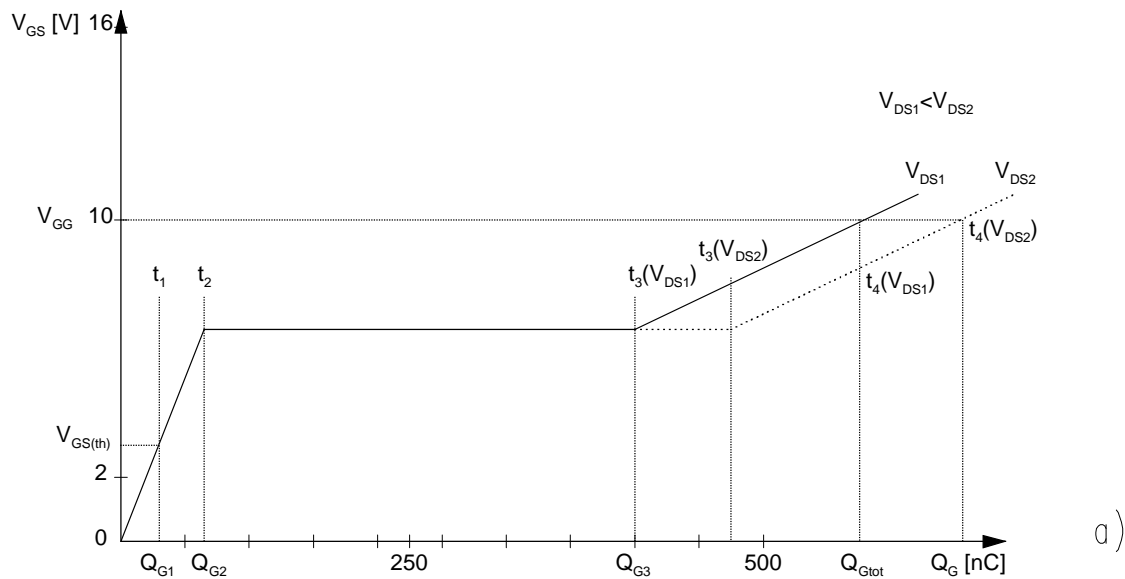


Figure 1.12 a) Gate-source voltage characteristic ( $V_{GS}$ ) of a power MOSFET dependent on the gate charge  $Q_G$  (gate charge characteristic)  
 b) Low-signal capacitances of a power MOSFET

### Turn-on: switching interval $0 \dots t_1$ (blocked transistor)

Gate current will be triggered by applying a control voltage.

Up to the charge quantity  $Q_{G1}$  the current  $i_G$  solely charges the gate capacitance  $C_{GS}$ . The gate voltage  $V_{GS}$  rises. As  $V_{GS}$  is still below the threshold voltage  $V_{GS(th)}$ , no drain current will flow during this period.

### Turn-on: switching interval $t_1 \dots t_2$ (rise of drain current)

As soon as  $V_{GS}$  has reached  $V_{GS(th)}$ -level at  $t_1$ , the transistor is turned on, first passing the *active region* (see chapter 1.2.2.1).

Drain current rises to  $I_L$ -level (ideal free-wheeling diode) or even exceeds  $I_L$  - as indicated in Figure 1.11a for a real free-wheeling diode. Similarly,  $V_{GS}$ , which is connected to the drain

current in the active region by the transconductance  $g_{fs}$  with  $I_D = g_{fs} * V_{GS}$ , will increase up to the value  $V_{GS1} = I_D/g_{fs}$  (time  $t_2$ ).

Since the free-wheeling diode can block the current only at  $t_2$ ,  $V_{DS}$  will not drop considerably up to  $t_2$ .

At  $t = t_2$  charge  $Q_{G2}$  has flown into the gate.

### **Turn-on: switching interval $t_2...t_3$ (transistor during turn-on)**

When the free-wheeling diode is turned off,  $V_{DS}$  will drop almost to on-state value  $V_{DS(on)}$  by time  $t_3$ . Between  $t_2$  and  $t_3$  drain current and gate-source voltage are still coupled by transconductance; therefore,  $V_{GS}$  remains constant. While  $V_{DS}$  is decreasing, the Miller capacitance  $C_{GD}$  is recharged by the gate current  $i_G$  with the charge quantity ( $Q_{G3}-Q_{G2}$ ). By  $t = t_3$  charge  $Q_{G3}$  has flown into the gate.

### **Turn-on: switching interval $t_3...t_4$ (ohmic characteristic area)**

At  $t_3$  the transistor is turned on, its curve has passed the pinch-off area to enter the ohmic area.  $V_{GS}$  and  $I_D$  are no longer coupled by  $g_{fs}$ .

The charge conducted to the gate ( $Q_{Gtot}-Q_{G3}$ ) at this point affects a further increase of  $V_{GS}$  up to the gate control voltage  $V_{GG}$ . Since the drain-source on-resistance  $R_{DS(on)}$  depends on  $I_D$  and  $V_{GS}$ , the on-state voltage  $V_{DS(on)} = I_D * R_{DS(on)}$  may be adjusted to the physical minimum by the total charge quantity  $Q_{Gtot}$  conducted to the gate.

The higher the drain voltage  $V_{DD}$  (or commutation voltage), the bigger the charge  $Q_{Gtot}$  required to reach a certain gate-source voltage, see Figure 1.12.

### **Turn-off**

During turn-off the described processes are running in reverse direction; the charge  $Q_{Gtot}$  has to be conducted out of the gate by the control current.

For approximations to determine the gate charge quantity required for turn-off, the gate charge characteristic in Figure 1.12 may be used.

The further the specific transistor application deviates from the „hard switch“-application described, the more the step-form of the gate-source voltage blurs. The intervals „decoupled“ by the free-wheeling diode during hard switching will then more or less merge into one another, which requires a more complex explanation of the switching behaviour. [278].

The above-mentioned description may be applied to IGBTpower modules by analogy. The switching behaviour can be determined correspondingly by the gate charge characteristic also indicated in the datasheets.

Since an IGBTgate is mostly switched between a positive and a negative gate voltage, also a certain charge quantity is required to switch the gate capacitance between 0V and  $V_{GG}$ . Therefore, the gate charge characteristic has to be extended as depicted in Figure 1.13. to calculate the total gate charges.