

- a) ...GA...: single switch, consisting of IGBT and hybrid inverse diode (as for MOSFET modules, here and in the other configurations, mostly just a parasitic inverse diode). In case of external bridge circuits, the inverse diodes are mutually acting as free-wheeling diodes.
- b) ...GB...: dual module (halfbridge module) consisting of two IGBTs and hybrid diodes (free-wheeling diodes)
- c) ...GH...: H-bridge with two arms consisting of IGBTs and free-wheeling diodes
- d) ...GAH...: asymmetrical H-bridge with two diagonal IGBTs with hybrid inverse diodes (free-wheeling diodes) and two free-wheeling diodes across the other diagonal.
- e) ...GD...: 3-phase bridge (Sixpack, inverter) with three arms consisting of IGBTs and free-wheeling diodes
- f) ...GAL...: chopper module with IGBT, inverse diode + free-wheeling diode on the collector side
- g) ...GAR...: chopper module with IGBT, inverse diode + free-wheeling diode on the emitter side
- h) ...GDL...: 3-phase bridge "GD" with chopper "GAL" (brake chopper)
- i) ...GT...: Tripack-module with three pairs of switches
- j) ...GAX... single switch with series diode on the collector side (reverse blocking switch)
- k) ...GAY... single switch with series diode on the emitter side (reverse blocking switch)
- l) ...GBD... dual module with series diodes (reverse blocking switch)
- m) ...B2U-diode rectifier and IGBT-H-bridge
- n) ...B2U-diode rectifier and IGBT-inverter (three-phase-bridge)
- o) ...B6U-diode rectifier and IGBT-chopper "GAL" (IGBT and free-wheeling diode on the collector side)
- p) ...B6U-diode rectifier and IGBT-H-bridge
- q) ...B6U-diode rectifier and IGBT-inverter (three-phase-bridge)
- r) ...B6U-diode rectifier, IGBT-chopper "GAL" and IGBT-inverter (three-phase-bridge)

The SEMIKRON code designation system for SEMITRANS-IGBT and MOSFET modules is referred to in chapter 1.4.4; for SKiiPPACK, MiniSKiiP and SEMITOP see chapter 1.5.

1.4.2.2 *Heat dissipation capability*

In order to guarantee optimal utilization of the theoretical current capability, generated power losses have to be conducted safely and straightforwardly through the connection and isolation layers to the heatsink.

Figure 1.47 shows the internal characteristics of a module which affect the capability to dissipate heat (internal thermal resistance R / internal thermal impedance Z), which determines the maximum losses in the module (current, switching frequency, voltage,...) together with cooling and ambient conditions.

The R-C elements shown in Figure 1.47, which are assigned to certain structural elements, are not meant to give an exact reflection of the physical heat conditions, but are only to illustrate the vertical flow of power and the temperature drop from the chip to the heatsink. The thermal resistances R_{th} characterize the static state, therefore they may be assigned to the structural elements.

However, capacitances replace physical elements, and may be gained by the transformation of real heat capacitances from volume elements (characterized by volume and specific heat) as opposed to a common thermal reference potential.

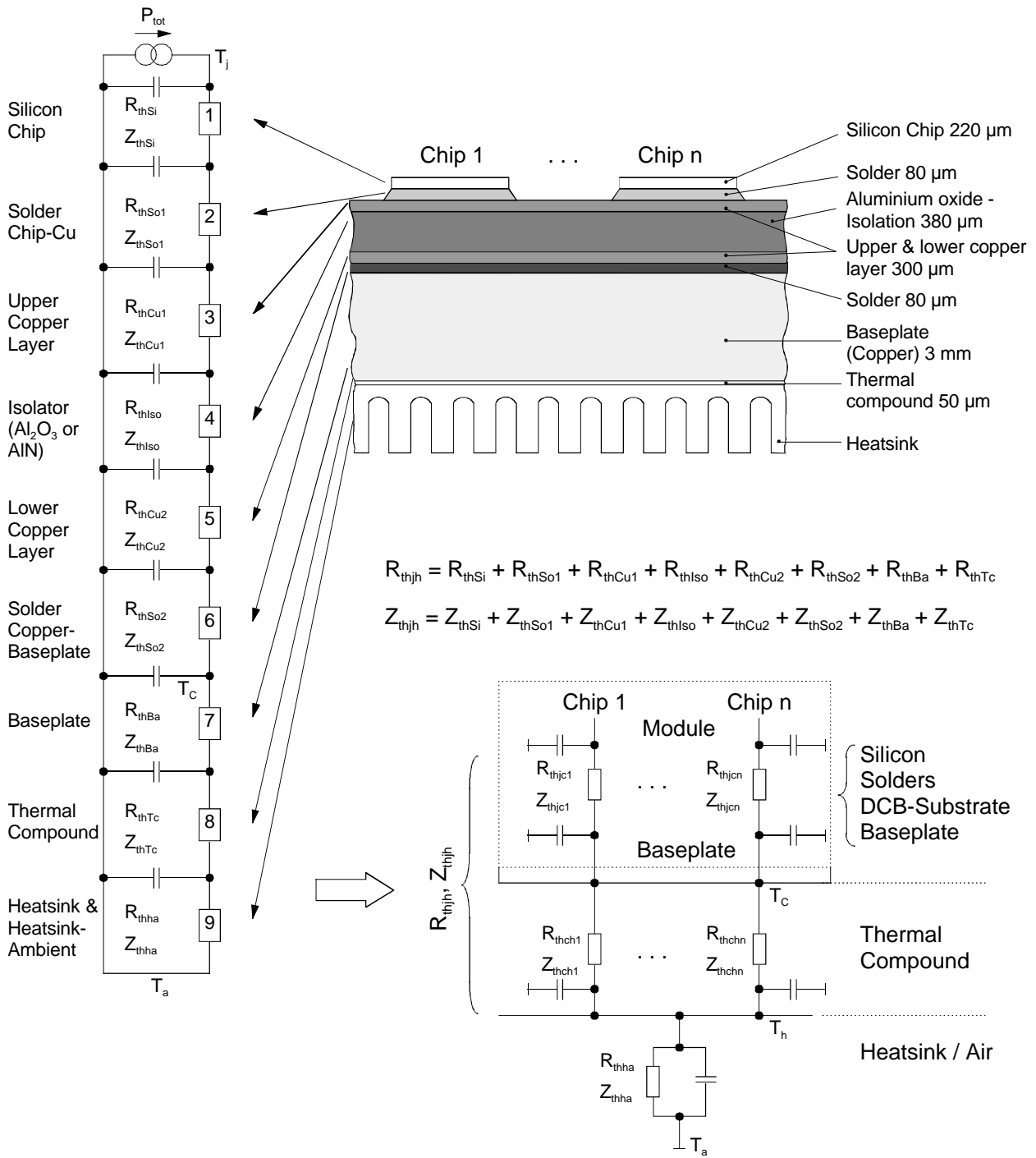


Figure 1.47a Basic structure of a power module with DCB illustrating the influences on heat dissipation

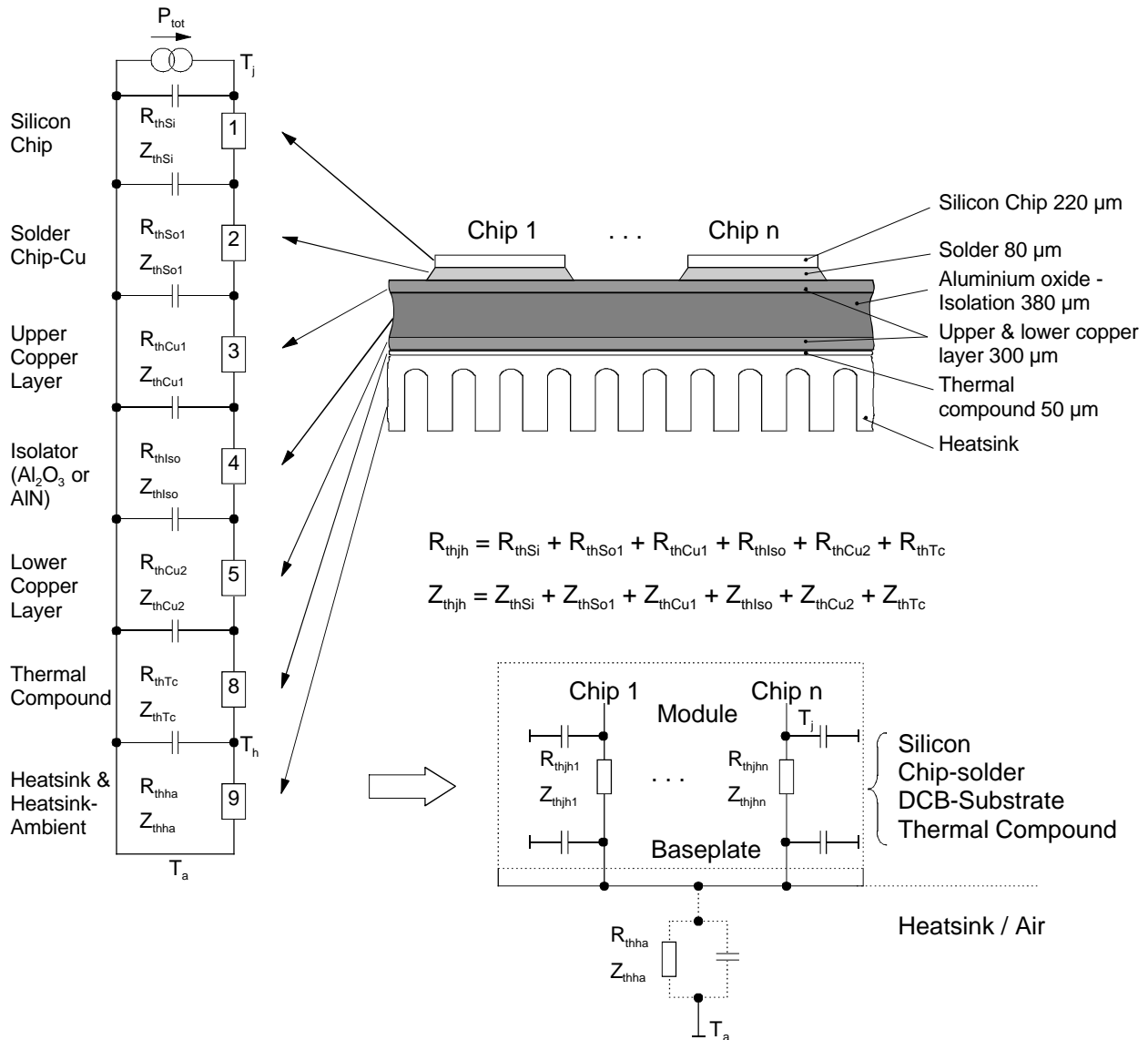


Figure 1.47b Basic structure of a power module with DCB without base plate illustrating the influences on heat dissipation

The quality of the dissipation of total power losses P_{tot} generated in chips during forward on-state and blocking state and during switching can be expressed by a minimized temperature drop

$$\Delta T_{jh} = T_j - T_h$$

from chip (chip temperature T_j) to heatsink (heatsink temperature T_h). It is quantified as thermal resistance R_{thjh} (stationary) or thermal impedance Z_{thjh} (transient).

Figures 1.47 and 1.48 illustrate the internal influences of the module on R_{thjh} and Z_{thjh} :

- chip (surface, thickness, geometry and position),
- structure of the DCB-substrate (material, thickness, top side structure),
- material and quality of connections between chip and substrate (solder, adhesive,...),
- existence of a base plate (material, geometry),
- backside soldering of the substrate to the base plate (material, quality),
- assembly of the module (surface qualities/ thermal contact to the heatsink, thickness and quality of thermal paste or thermal foil).

This list is still to be supplemented by the mutual heating of chips (thermal coupling) in complex power modules.

For modules with base plate the external thermal resistance or impedance (base plate-heatsink) is indicated with R_{thch} or Z_{thch} , respectively, in contrast to the “internal“ resistance R_{thjc} or impedance Z_{thjc} (chip-base plate):

$$R_{thjh} = R_{thjc} + R_{thch}$$

$$Z_{thjh} = Z_{thjc} + Z_{thch}$$

This difference cannot be made for modules without base plate.

Figure 1.48 indicates the R_{thjc} -shares of the above-mentioned influences for the most common module structures of today described in chapter 1.4.2 with Al_2O_3 -direct-copper-bonding (DCB)-substrates and Cu-base plates as well as for modules with insulated metal substrates (IMS).

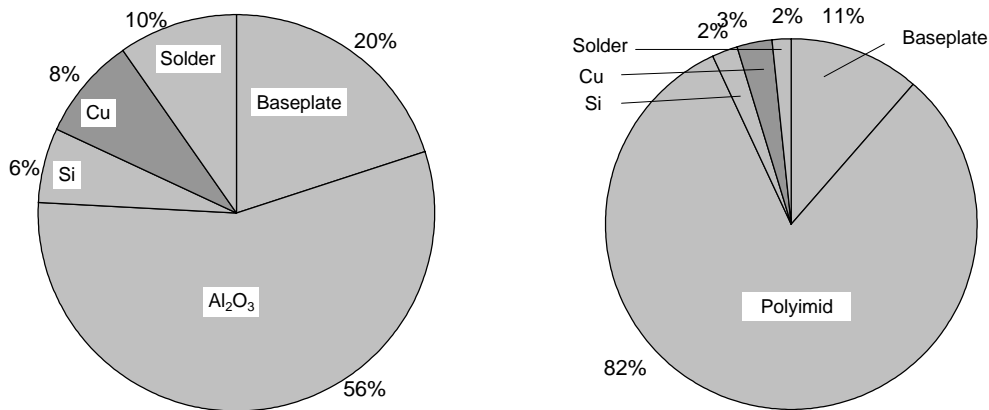


Figure 1.48 Influences on the internal thermal resistance of a 1200 V-power module, chip surface 9 mm * 9 mm [194]
 a) For DCB-substrates (Al_2O_3) on a Cu-base plate
 b) For IMS

The main share of thermal resistance is allotted to *internal module insulation* (the alternative of external insulation with foils or something similar would result in a deterioration of insulation by an even further 20 %...50 %!). Compared to Al_2O_3 with a purity of 96 % (heat conductivity $\lambda = 24 \text{ W/m}\cdot\text{K}$), which is applied as a standard in common DCB-modules, improvements can be made by using highly pure (99 %) Al_2O_3 ($\lambda = 28 \text{ W/m}\cdot\text{K}$) or aluminum nitride (AlN, $\lambda = 150 \text{ W/m}\cdot\text{K}$). In modules with high isolation voltages (thicker isolation ceramics) especially, AlN, which is still very expensive, is preferred nowadays.

Despite the high thermal conductivity of its material (Cu: $\lambda = 393 \text{ W/m}\cdot\text{K}$), the base plate also contributes to a considerable share of thermal module resistance due to its thickness (2.5...4.5 mm). This share may be only partly reduced, since a reduction of the base plate thickness would also bear the consequences of reduced temperature spreading and, thus, reduction of the area through which the heat passes under the chips. In modules without base plate the lack of heat spreading in Cu is compensated by missing thermal resistances of base plate and rear-side soldering.

Furthermore, on condition there is a suitable assembly technology (DCB is pressed on to the heatsink over wide areas), the chips will adhere closer to the substrate compared to constructions

with base plate, since base plate and heatsink will never fully contact each other because of unavoidable unevenness generated during the soldering process and, since the base plate is only fixed to the heatsink by means of pressure screws positioned at the margins (Figure 1.49).

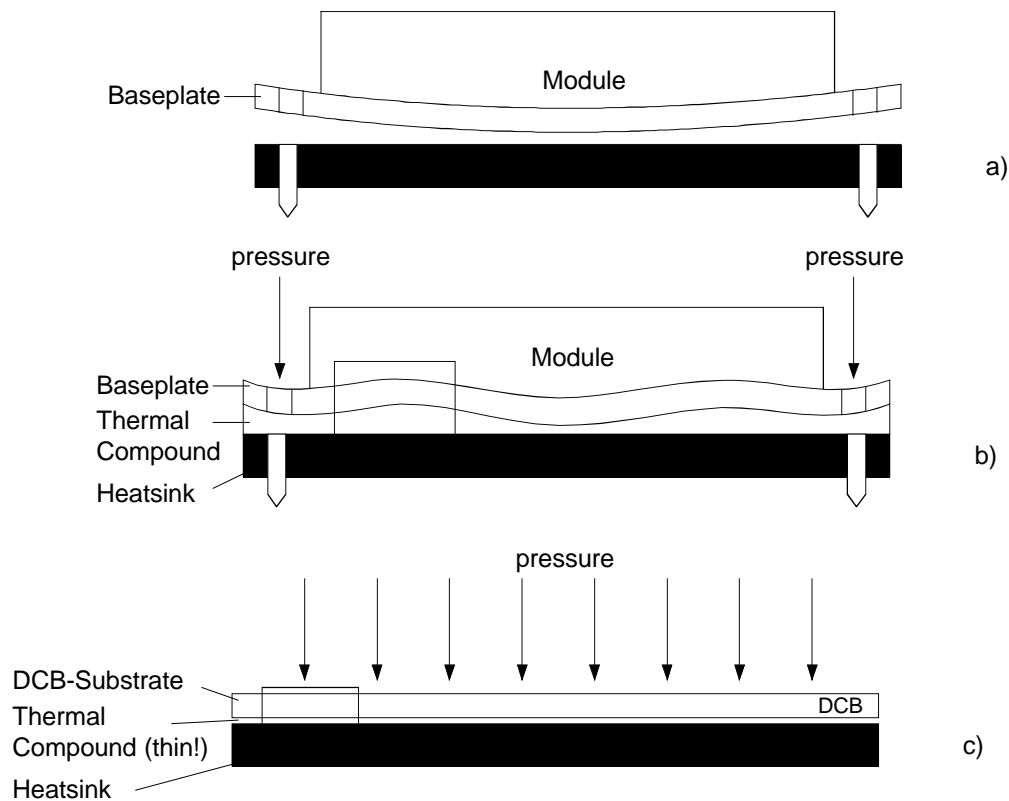


Figure 1.49 Problems arising through contact of power module to heatsink
 a) Module with base plate before mounting (base plate with convex bending)
 b) Module with base plate after mounting (strongly exaggerated!)
 c) DCB-module without base plate (e.g. SEMITOP, SKiiP, MiniSKiiP)

Another factor that must not be neglected is the thermal resistance of the chip-substrate and (if applicable) substrate-base plate connections, which are produced as *solder connections* (e.g. $\lambda = 75 \text{ W/m}\cdot\text{K}$). The share of this resistance may be reduced by about 50 %, in cases where there is no base plate.

The thermal resistance share of *metal substrate areas* (Cu: $\lambda = 393 \text{ W/m}\cdot\text{K}$) depends mainly on the structure of the top side copper surface, which is used as chip carrier and internal electrical connection system of the module. While the lateral heat flow in the lower copper layer is practically not impaired, spreading of heat is limited by the geometrical dimensions of the copper layers under the chips. It had been determined in reference [194] that R_{thjc} of a chip of $6.5 \text{ mm}\cdot 6.5 \text{ mm}$ on a Al_2O_3 -DCB-ceramic substrate exceeds the value of a ten times as big copper area by about 15 %, provided the chip and copper areas are identical.

The thermal resistance share of *silicon chips* increases proportionally to the *thickness of the chips*, which is determined by forward blocking voltage and chip technology. Moreover, the *chip area* determines the area through which the heat passes between chip and base plate or heatsink.

On the one hand, the thermal resistance is reduced by increased chip areas due to a bigger area through which the heat passes. On the other hand, an increase of the area/ circumference ratio of

the chip will increase the influence of the thermal coupling of the heat flowing inside the chips on the thermal resistance, heat spreading will be diminished. Both opposite tendencies will lead to dependency of the thermal resistance R_{thjc} on the chip area A_{ch} shown in Figure 1.50.

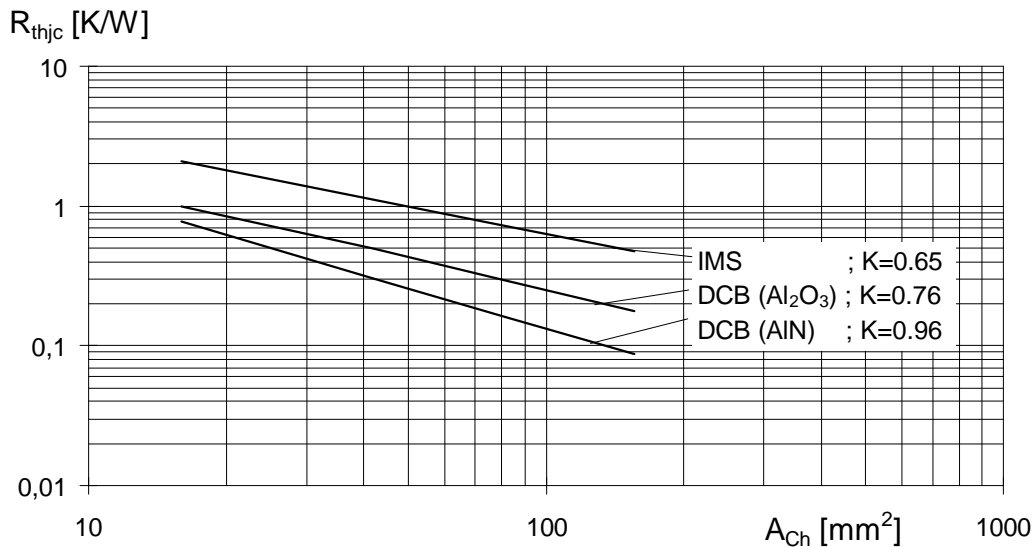


Figure 1.50 Dependency of thermal resistance R_{thjc} on chip area A_{ch} [194]

The dependency of R_{thjc} on A_{ch} is almost linear, when the total heat conductivity of the substrate (e.g. AlN-DCB) is high, since the chip area will hardly influence heat spreading. The worse the heat conductivity of the ceramics, the higher the non-linearity of the R_{thjc} -dependency on A_{ch} . Therefore, the maximum power loss density in the chips (chip utilization) will be drastically reduced by increasing the chip areas in like assemblies.

This correlation is also valid for the influence of module mounting to the heatsink, which is done with thermal paste or thermal foils. With a value of $\lambda = 0.8 \text{ W/m}\cdot\text{K}$ the heat conductivity of this layer is relatively low, which will cause a thermal transient resistance R_{thch} between module base plate and heatsink. Besides the thickness d of the thermal paste layer, the R_{thch} -share in the thermal resistance R_{thjh} between chip and heatsink will also rise with increasing chip area.

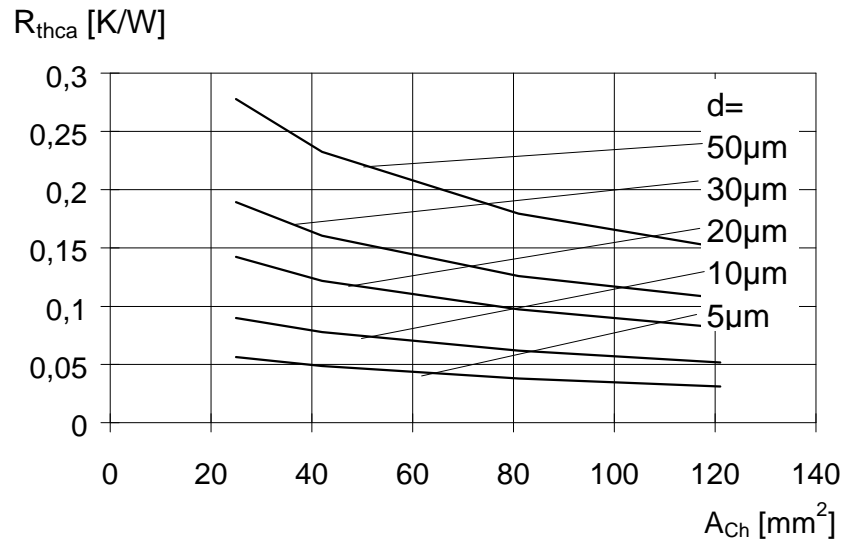


Figure 1.51 Thermal resistance of thermal paste R_{thca} of a DCB-substrate (Al_2O_3) according to [279] and [194]

First of all, Figure 1.51 shows the influence of an optimal mounting technology (thin thermal paste layer) on thermal parameters.

Secondly, it shows that thermal limits are set to the use of bigger chips to increase power output; the thermal resistance share R_{thjh} of thermal paste, for example, will amount to approximately 30 % at an application thickness of $30 \mu\text{m}$ for a 50A-IGBT-chip ($9 \text{ mm} * 9 \text{ mm}$).

Currently, the maximum chip sizes used in power modules are between 30 mm^2 (IMS) and 150 mm^2 (Al_2O_3 -DCB). Higher power output can be reached by decentralization of heat sources (paralleling of a maximum number of chips).

For the sake of a small geometry of the modules, more or less intensive *thermal coupling* of chips has to be accepted, which is due to the tight arrangement of transistor and diode chips.

According to the calculations in reference [194] an increase of the chip temperature caused by thermal coupling e.g. on a Al_2O_3 -DCB-ceramic substrate should always be taken into consideration, if the distance a of the chips equals:

$$a = 0.58 \cdot \sqrt{A_{ch}}$$

As already mentioned above, apart from the static behaviour of power modules the *dynamic thermal behaviour*, which is characterized by the thermal impedance Z_{th} , is also of major importance.

Figure 1.52 shows the characteristic of the thermal impedances Z_{thjc} of a module with Al_2O_3 -DCB-substrate for different chip areas versus time.