

Figure 1.52 Thermal impedances Z_{thjc} of a module with Al_2O_3 -DCB-substrate for different chip areas versus time [194]

For the given module structure the Z_{th} -characteristics for different chip areas may be shifted against each other, i.e. the absolute values will change proportionally to the chip area, however, without influencing the time constants of the exponential functions.

Accordingly, thermal impedances for different chip areas may be calculated similarly to the thermal resistances in a given structure by

$$Z_{thjc1}(t)/Z_{thjc2}(t) = R_{thjc1}/R_{thjc2} = (A_{Ch2}/A_{Ch1})^K.$$

Hereby, the exponent K , as a parameter indicating the influence of heat accumulation effect, may be determined from Figure 1.50 [194].

1.4.2.3 Isolation voltage/ partial discharge stability [275]

Advancing in the high-voltage application range will result in increasing demands on IGBT-modules for high isolation voltages and a high partial discharge stability.

Isolation and partial discharge stability are dependent on the thickness, material and homogeneity of the insulation on the chip bottom and the case materials and, sometimes, on the chip arrangement too.

The current transistor modules are subject to isolation test voltages between $2.5 \text{ kV}_{\text{eff}}$ and $9 \text{ kV}_{\text{eff}}$, applied to every module during production.

Figure 1.53 shows the maximum attainable isolation voltages for different isolation substrates and today's standard substrate thicknesses d .

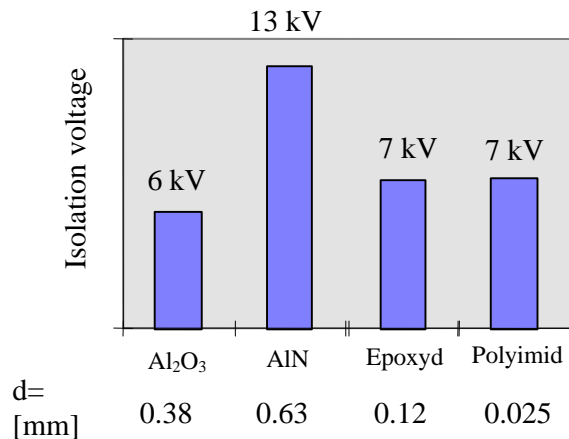


Figure 1.53 Isolation voltages for different isolation substrates with DCB, IMS and TFC

1.4.2.4 Power cycling capability

Power cycling at frequencies below approximately 3 kHz, especially at duty cycle operation, such as prevails in traction, lift and pulse applications, will expose the internal connections in a module to temperature cycling, such connections being:

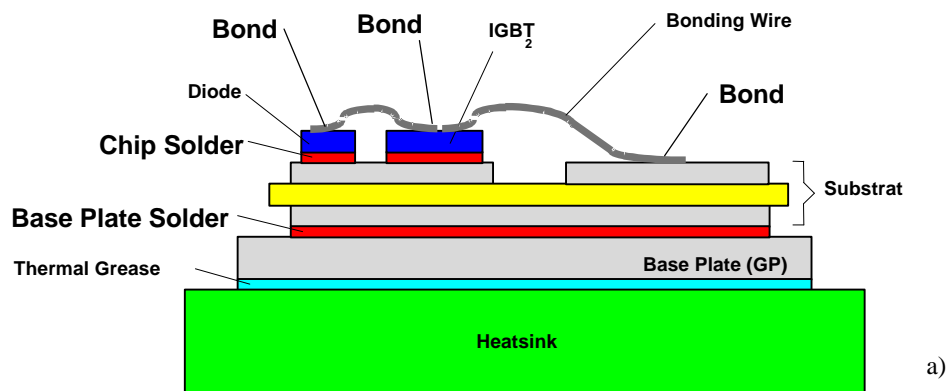
- bonded joints,
- underside soldering of chips,
- solder connection of DCB and base plate,

as well as substrate lamination (Cu on Al₂O₃ or AlN).

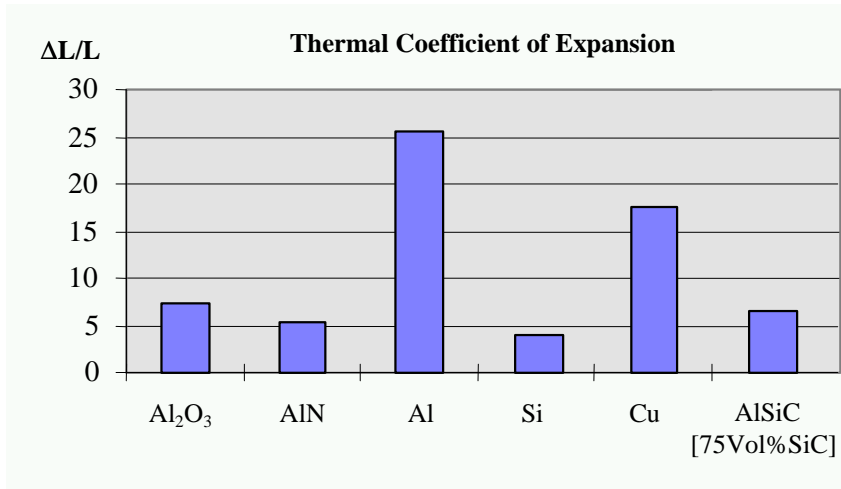
The different coefficients of the length expansion of the layers cause thermal stress during production and operation, which will finally lead to wear and tear of the material; module load life (number of possible switching cycles) will be shortened when the amplitude of the chip temperature fluctuation increases during these cycles.

Test procedures are dealt with in chapter 2.7; the correlation of module life and temperature cycling amplitude will be explained in chapter 3.2.3.

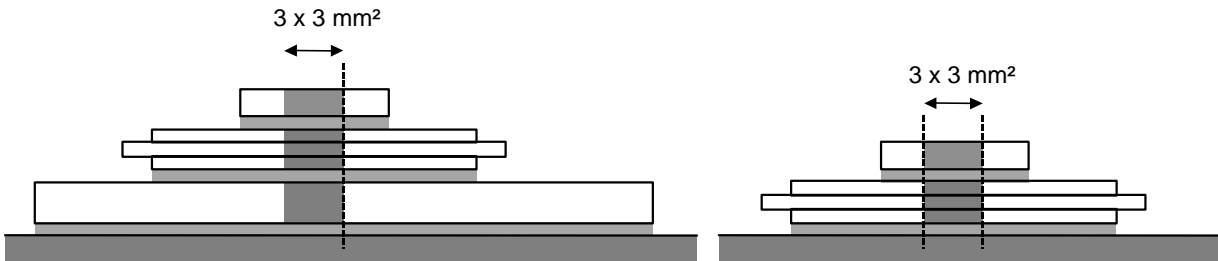
Figure 1.54a explains the structural details relevant to the module life of an IGBT.



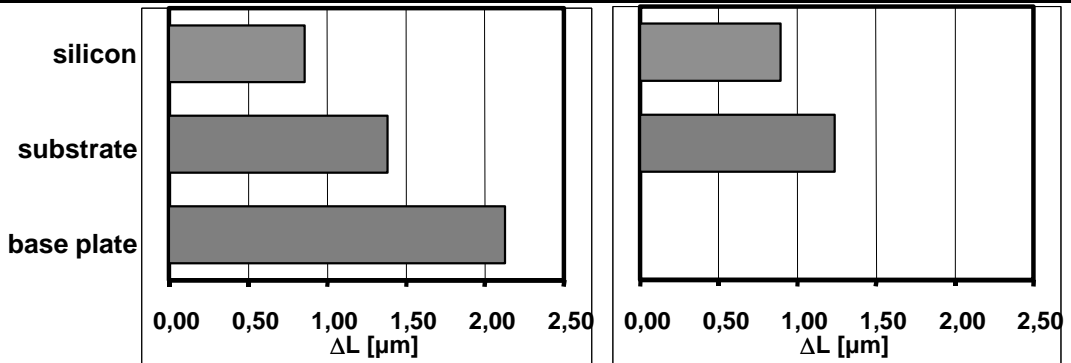
a)



b)



System:	standard 34mm module 0,38mm-Al ₂ O ₃ / Cu base plate			SKiiP pressure system 0,38mm-Al ₂ O ₃		
Results:	T-Tkk [K]	ΔL/L [1E-6/K]	ΔL [μm]	T-Tkk [K]	ΔL/L [1E-6/K]	ΔL [μm]
silicon	69,7	4,1	0,86	62,6	4,1	0,77
substrate	55,4	8,3	1,38	48,3	7,8	1,13
base plate	40,5	17,5	2,13	—	—	—



c)

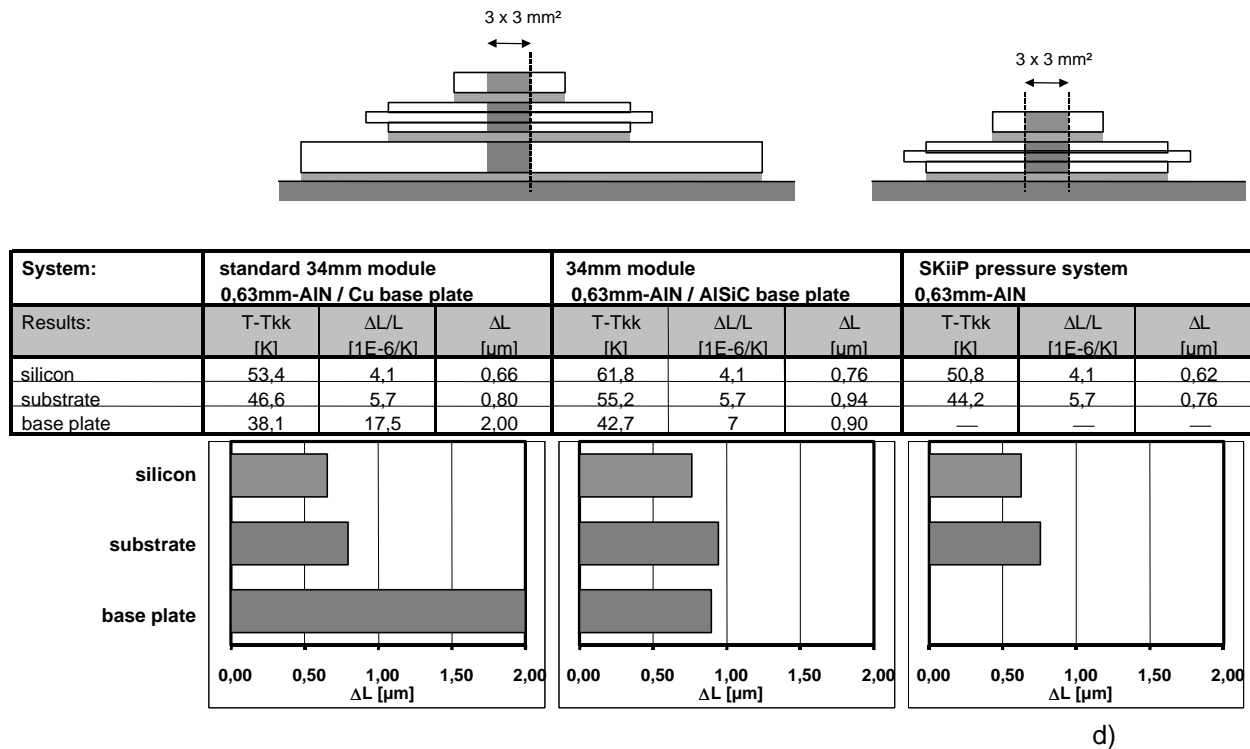


Figure 1.54 Thermal expansion in a power module

- Standard assembly of module with base plate
- Thermal coefficient of expansion
- Comparison: assembly with and without copper base plate; Al_2O_3 – substrate
- Comparison: assembly with and without copper/AlSiC base plate; AlN - substrate

Figure 1.54 makes clear that the *solder connection of the substrate to the copper base plate* is most critical, since it is the most extensive connection - medium differences in the expansion coefficients of the adjacent materials provided. Therefore, high-quality solders and sophisticated soldering procedures have to be applied in order to avoid deformation and destruction of the substrate also in case of high temperature cycling amplitudes.

Moreover, often the DCB-substrates are divided up to keep the absolute difference of the expansion coefficient as small as possible by reducing the solder areas.

Other, lately developed module types are replacing copper by a material with a smaller expansion coefficient (such as AlSiC), see chapter 1.5.4 and [206].

It is also shown in Figure 1.54 that modules with AlN-DCB are especially sensitive, because the expansion coefficient of AlN is very similar to that of the chip silicon, but there are greater deviations to copper than with Al_2O_3 . Therefore, today's modules with AlN-DCB and Cu-base plate cannot completely utilize the actual material performance with reference to the corresponding datasheets.

It has become very obvious that one of the main causes for wear and tear can be eliminated by doing without a base plate and the necessary soldering, as long as the heat transfer from the substrate to the heatsink can be sufficiently ensured and the disadvantages of reduced heat spreading can be compensated. This has been realized with SKiiP, MiniSKiiP, SEMITOP and SKiM technologies (see chapter 1.5).

The temperature cycling capability of the *soldering of the chips to the substrate* can be improved by

- use of AlN-substrates with less deviation of the expansion coefficient to Si than Al₂O₃,
- substitution of soldering by low-temperature connections; the connection between chips and substrate is realized by sintering silver powder at comparably low temperatures (150...200°C), which will minimize thermal stress among the materials during production.

Bond connections. Also the lifetime of the connection between bond wire and chip is influenced decisively by the difference in thermal coefficients of expansion.

Silicon shows a relative slight length expansion (4.7 ppm/K) during power cycling. However, the Al-metallization of the emitter and gate contacts which are stressed by the same temperature fluctuations shows a considerable higher relative length expansion (23 ppm/K).

The stress inside of the metallization caused by this difference in expansion effects a rearrangement of the crystal grains. This process is called „reconstruction“.

The reconstruction - mostly identifiable by an optical dispersive surface – leads to the destruction of the bond wire connection [304]. Reconstruction of Al-contact metallization can be reduced by a polyimide-cover.

The lifetime of the bond connection on the chip contact area is increased considerably using bond covers. However, another type of failure occurs. The mechanical deflection of the bond wire during thermal alternating stress caused by the different thermal expansion of substrate and Al-wire leads to a fracture of the bond wire nearby the „bond-heel“ on the PCB-sided juncture since the chip-sided „bond-heel“ is mechanically strengthened by the polyimide cover.

Bond wire failures are mostly observed in lifetime tests whereas the failure is caused really by ageing of the solder layer. Caused by growing cracks in solder layer the thermal resistance increases and effects a increasing chip temperature and thus a higher stress for both the bond connection and chip solder layer. Finally, this positive feedback leads to a failure.

In any case, the ageing of solder connection has to be investigated at failure analysis. Using today's technologies solder connections and bond connections have nearly the same lifetime at cycles with high temperature ripples ($\Delta T \approx 100\text{K}$).

In state-of-the-art power cycling test equipment forward voltage drop and thermal resistance of power devices are measured and recorded. So, both degeneration of solder layer and bond connection failures (steps in forward voltage drop characteristic) can be observed.

Bond connections in IGBT and diode-disc cells have been replaced by pressure contacts with a higher temperature cycling capability due to pressure contact technology. Processes for transferring this direct pressure contact technology to power modules are also currently being developed.

1.4.2.5 Internal low-inductive structure

With the example of a halfbridge module, Figure 1.55 shows the most important internal parasitic inductances of a module, resulting from the necessary connections among the chips and to the module terminals (bond wires, internal connections).

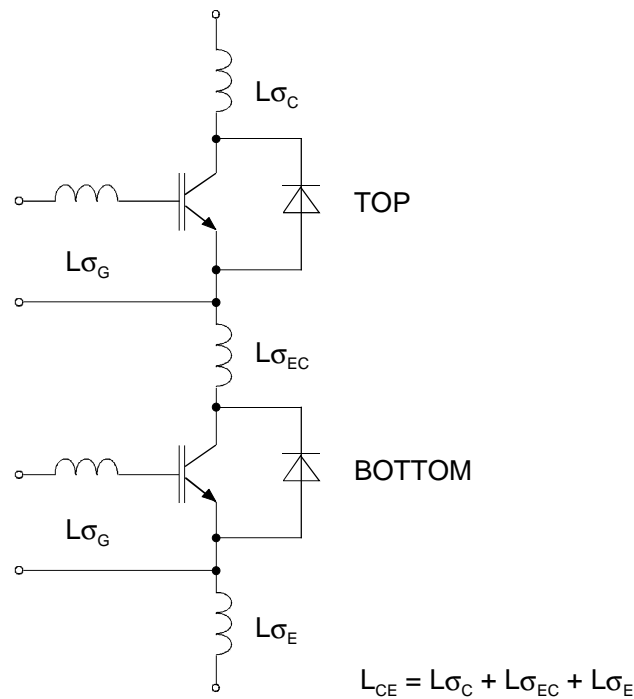


Figure 1.55 Parasitic inductances in a dual IGBT-module
 $L_{\sigma G}$: parasitic gate inductances
 $L_{\sigma C}$: parasitic TOP-collector inductance
 $L_{\sigma EC}$: parasitic inductance between TOP-emitter and BOTTOM-collector
 $L_{\sigma E}$: parasitic BOTTOM-emitter inductance
 L_{CE} : total parasitic TOP-collector-BOTTOM-emitter inductance

Minimization of these inductances, which induce overvoltages during turn-off and cause a di/dt reduction during turn-on as well as inductive coupling of control and power circuit, will directly affect the performance of power modules.

Moreover, parasitic inductances in modules with internally paralleled chips may cause unequal dynamic performance of the chips and oscillations between the chips.

Chapter 3.4.1 gives details on these correlations.

1.4.2.6 Internal structure-adapted to EMC

The short rates of rise of current and voltage within the ns-range realizable with MOSFET- and IGBT-modules generate electromagnetic interference with frequencies far beyond the MHz-range. Therefore, the parasitic elements typical of the internal and out-leading paths of propagation in the module exert considerable influence on the interference voltages generated.

Suitable isolation materials, small coupling areas or conductive shields can reduce, for example, asymmetrical interferences [193].

In addition to that, the internal connections in the module have to be of such a structure, that excludes failures caused by outer stray fields or transformatory couplings into control lines.

Another aspect of electromagnetic compatibility is the “earth current“, i.e. the current $i_E = C_E \cdot dv_{CE}/dt$ that flows due to the capacitance C_E of the isolation substrate caused by the dv_{CE}/dt generated in the IGBTs during switching via the earthed heatsink to the earth connector.

This earth current is identified as earth-leakage current by line monitors; its permissible maximum value is to be limited to 0.1...5 % (1 % anticipated) of the nominal output current as soon as the new EN 50178 comes into effect.

Accordingly, the permissible switching speed will increase proportionally to the decrease of capacitance of the isolation substrate.

Figure 1.56 compares the capacitances of the most commonly used substrates with respect to their standard thicknesses. The deviating dielectric constants and the standard thicknesses depending on thermal conductivity (thickest substrate material is AlN with 630 μm , thinnest substrate is required in IMS-structures with 120 μm for epoxy isolation and 25 μm for polyimide isolation) result in respectively differing capacitances C_E and, thus, in different limits of the maximum switching velocity dV_{CE}/dt for the maximum tolerable earth current i_E .

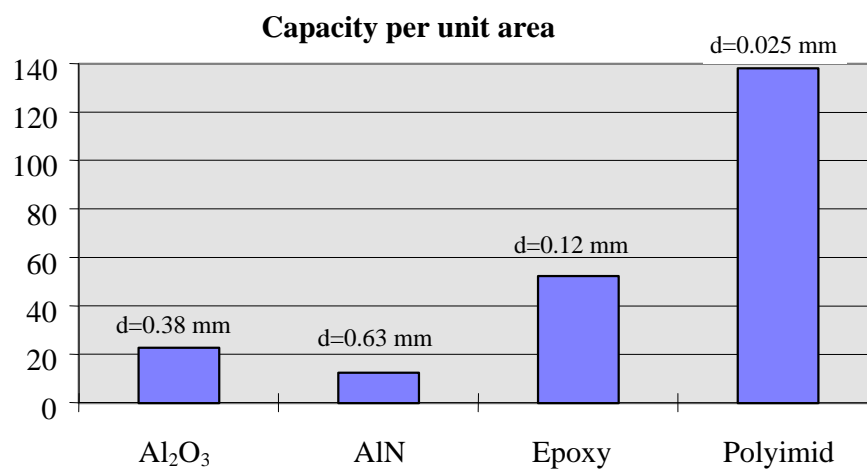


Figure 1.56 Capacitance per unit area for different isolation substrates

1.4.2.7 Defined safe behaviour in case of module failure

In the case of module failure (probably caused by use of wrong driver) the total energy stored in the DC-link capacitors will be transferred, for example, in a voltage-supplied circuit within the module case. After melting the bond wires this energy is mainly stored in the generated plasma, which allows the module to explode.

In conventional transistor modules this may cause circuit interruption, short-circuit of the main terminals or even bridging of the isolation; plasma and particles of the case might be spread over the module surroundings with high kinetic energy.

With the proper case construction, the dangers involved may be limited and the particles spread are guided in a defined direction.

The latest developments in this field guarantee, for example, that up to a defined energy level of e.g. 15 kJ no particles will leave the module; even at 20 kJ the case might break, but no solid metal particles would be hurled out [196].

1.4.2.8 Non-polluting recycling

Today's power modules usually exclude toxic materials (e.g. BeO) and the number of materials used is kept as low as possible.

Case and other materials are flame-resistant and must not release toxic gas during burn-out (UL-specification).