

### 2.2.3 Diagrams

Following the sequence of the datasheets, this chapter will give some hints concerning MOSFET datasheet diagrams. In the case where the diagram concerned is detailed in other chapters, this will be referred to.

#### Rated power dissipation $P_D$ of a MOSFET module versus case temperature $T_{case}$

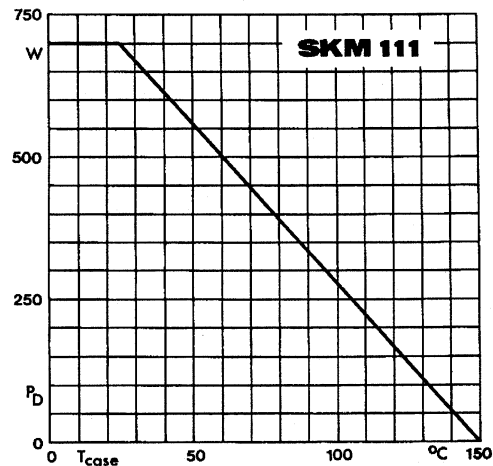


Figure 2.2 Rated power dissipation

Based on the rated power dissipation per MOSFET  $P_{D(25^\circ\text{C})} = (T_{jmax} - 25^\circ\text{C})/R_{thjc}$  which is limited to  $T_{case} = 25^\circ\text{C}$  per definition, the function depicted in the diagram describes derating at a higher case temperature.

#### Maximum safe operating area during pulse operation (SOA)

As explained in chapter 1.2.3 the MOSFET has to manage an almost rectangular characteristic  $i = f(u)$  between  $V_{DD}$  and  $I_L$  in the case of hard switching.

The SOA (Safe Operating Area)-diagrams indicate to what extent this may be realized during different operations without risk of destruction:

The SOA is terminated by the following parameters:

- maximum drain current (horizontal termination);
- maximum drain-source voltage (vertical termination);
- maximum power dissipation or chip temperature (diagonal broken termination line in Figure 2.3);
- turn-on resistance (diagonal continuous termination line).

Figure 2.3 shows the maximum curve  $I_D = f(V_D)$  during switching and on-state for different pulse durations  $t_p$  at a double logarithmic scale.

It is important that the maximum ratings are valid at a case temperature  $T_c = 25^\circ\text{C}$  and for single pulses, which will not heat the MOSFET over the maximum chip temperature  $T_j = 150^\circ$ .

Although the lowest of the depicted diagonals represents the hyperbola of the maximum stationary power losses  $P_{tot}$ , MOSFET modules may only touch the linear characteristic area during switching operation. Analogous operation over a longer period of time is not permitted, since asymmetries due to spreading among the chips as well as negative temperature coefficients of the threshold voltages might cause thermal instability.

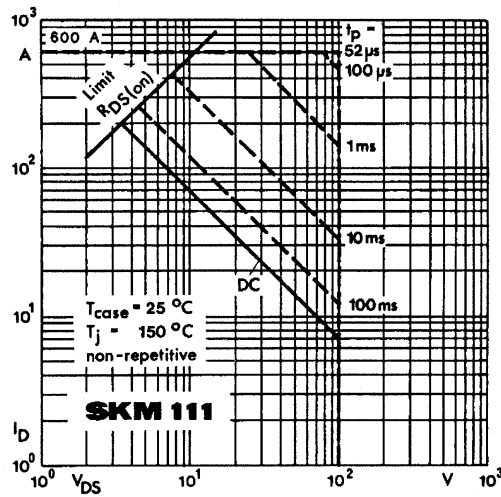


Figure 2.3 Maximum safe operating area  $I_D = f(V_{DS})$  during pulse operation (SOA)

**Forward output characteristic  $I_D = f(V_{DS})$**

Figure 2.4 shows the output characteristic (typical values) with parameter  $V_{GS}$  (also see chapter 1.2.2.1).

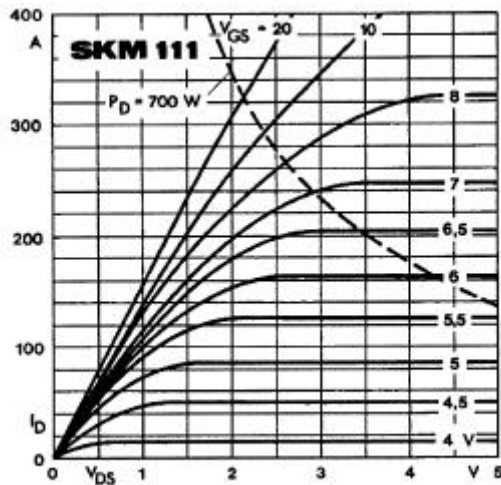


Figure 2.4 Typical MOSFET output characteristic  $I_D = f(V_{DS})$  with parameter  $V_{GS}$

**Transfer characteristic  $I_D = f(V_{GS})$**

The transfer characteristic (Figure 2.5) describes the behaviour of the MOSFET in the active operating area at  $V_{DS} = 25 \text{ V}$  (linear operation). The drain current is coupled with the gate-source voltage via  $I_D = g_{fs} * (V_{GS} - V_{GS(th)})$ .

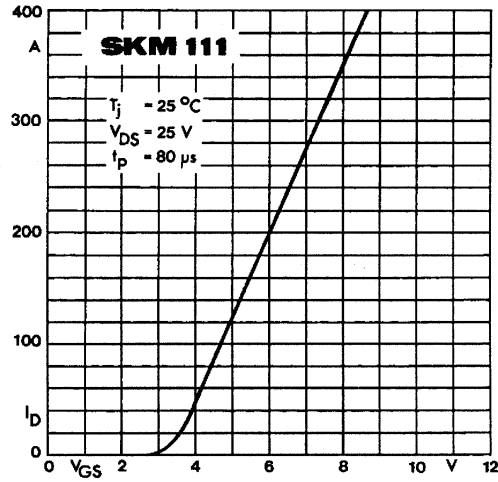


Figure 2.5 Typical transfer characteristic  $I_D = f(V_{GS})$

**On-resistance versus chip temperature**

see chapter 2.6

**Drain current derating versus case temperature**

see chapter 2.6

**Drain-source breakdown voltage versus temperature**

As shown in Figure 2.6 the drain-source breakdown voltage of a MOSFET increases linearly to the temperature. As the maximum rating indicated in the datasheets refers to  $T_j = 25^\circ\text{C}$ , deratings at low chip temperatures have to be accepted .

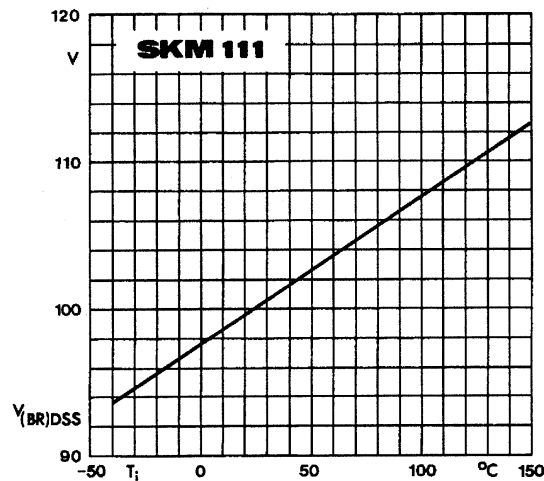


Figure 2.6 Drain-source breakdown voltage  $V_{(BR)DSS}$  versus  $T_j$

**Drain-source voltage derating versus rate of fall of drain current**

see chapter 3.1.1

**Internal capacitances versus collector-emitter voltage**

see chapter 1.2.3

**Gate charge characteristic**

see chapter 1.2.3

**Diode forward characteristic**

see chapter 1.2.2.1

**On-resistance versus drain current**

Figure 2.7 explains the relationship between on-resistance  $R_{DS(on)}$  and drain current  $I_D$  or gate-source voltage  $V_{GS}$  for a fully controlled MOSFET.

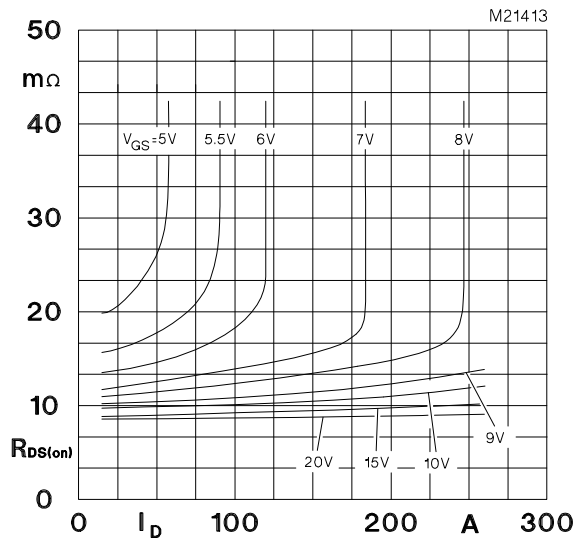


Figure 2.7 Typical characteristic of on-resistance  $R_{DS(on)}$  versus drain current  $I_D$  and gate-source voltage  $V_{GS}$

The on-resistance decreases with increase of the gate-source voltage. At any point of the curve, a slight increase of  $R_{DS(on)}$  together with the drain current has to be considered.

**Gate-source threshold voltage versus temperature**

Figure 2.8 shows three curves with typical and limit values characterizing the relationship between gate-source threshold voltage  $V_{GS(th)}$  and MOSFET chip temperature  $T_j$ .

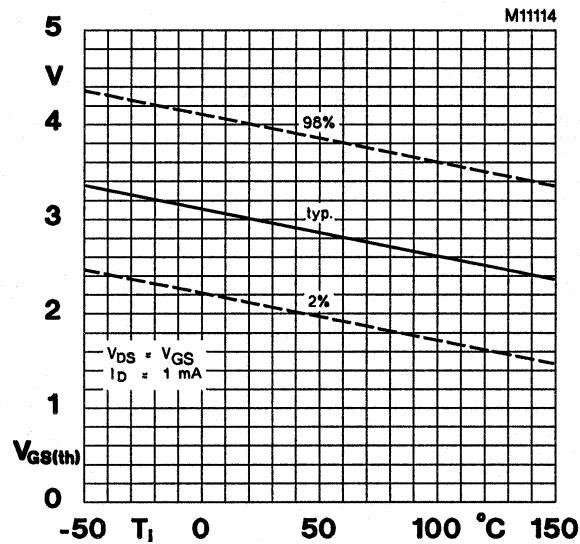


Figure 2.8 Gate-source threshold voltage  $V_{GS(th)}$  versus temperature

$V_{GS(th)}$  will decrease linearly when  $T_j$  increases. The temperature coefficient of the threshold voltage amounts to about  $-10 \text{ mV/K}$  within the temperature range of  $-50\dots+150^\circ\text{C}$ .

### Transient thermal impedances for IGBTs and free-wheeling diodes

see chapter 3.2

## 2.3 IGBT-modules [264], [265]

### 2.3.1 Maximum ratings

*IGBTs/ module structure*

#### Collector-emitter voltage $V_{CES}$ or $V_{CE}$

Maximum collector-emitter voltage with gate-emitter short-circuited ( $V_{GE} = 0$ )

Parameter: case temperature  $T_{case} = 25^\circ\text{C}$

#### Collector-gate voltage $V_{CGR}$

Maximum collector-gate voltage,

Parameters: external gate-emitter resistance  $R_{GE}$ ; case temperature  $T_{case} = 25^\circ\text{C}$

#### Continuous collector current $I_C$

Maximum direct current at collector output

Parameter: case temperature, e.g.  $T_{case} = 25^\circ\text{C}, 80^\circ\text{C}$ :  $I_{C@25^\circ\text{C}}, I_{C@80^\circ\text{C}}$

#### Peak value of a periodic collector current $I_{CM}$ or pulsed collector current $I_{Cpuls}$

Peak value of current at collector output during pulse operation

Parameters: pulse duration  $t_p$ , case temperature, z.B.  $T_{case} = 25^\circ\text{C}, 80^\circ\text{C}$  and pulse/ break ratio

#### Gate-emitter voltage $V_{GES}$ or $V_{GE}$

Maximum gate-emitter voltage

Parameter: case temperature  $T_{case} = 25^\circ\text{C}$