

SKiiPPACK no. 3

$$Z_{\text{thsa tot3}} = \sum_{v=1}^4 R_v \cdot [1 - \exp(-t/\tau_v)] + [(P_{\text{tot1}} + P_{\text{tot2}})/P_{\text{tot3}}] \cdot R_{\text{thaa2-3}} \cdot [1 - \exp(-t/\tau_{\text{aa2-3}})]$$

3.3.6.2 Liquid cooling

The following table contains the characteristics R_v and τ_v for thermal calculation according to the 4-time-constants-model for SKiiPPACKs on a standard water-cooled heatsink S1021450 with mutual water inlet/outlet, 50/50 % water-glycol-mixture at a coolant temperature of 50°C. Since the temperature T_s of the internal temperature sensor of the SKiiP is also available here as a reference point for the heatsink temperature T_h , the following definitions are valid:

$R_{\text{thsw tot}}$: stationary thermal resistance as a result of the temperature difference between temperature sensor (T_s) and coolant (T_w), with reference to the total power dissipation P_{tot} of the assembly.

$$R_{\text{thsw tot}} = \sum_{v=1}^4 R_v$$

$Z_{\text{thsw tot}}$: transient thermal impedance as a result of the temperature difference between temperature sensor (T_s) and coolant (T_w), with reference to the total power dissipation P_{tot} of the assembly.

$$Z_{\text{thsw tot}} = \sum_{v=1}^4 R_v \cdot [1 - \exp(-t/\tau_v)]$$

Coolant by-pass l/min	thermal characteristics (4-constants-model)									
	R_1 K/W	R_2 K/W	R_3 K/W	R_4 K/W	ΣR K/W	τ_1 s	τ_2 s	τ_3 s	τ_4 s	
2-fold SKiiPPACK										
6	1.942· 10 ⁻³	6.262· 10 ⁻³	3.785· 10 ⁻³	6.608· 10 ⁻³	1.860· 10 ⁻²	1.225· 10 ⁻¹	2.911	1.189· 10 ¹	5.196· 10 ¹	
10	1.942· 10 ⁻³	6.262· 10 ⁻³	4.402· 10 ⁻³	2.993· 10 ⁻³	1.560· 10 ⁻²	1.225· 10 ⁻¹	2.911	1.782· 10 ¹	1.131· 10 ²	
14	1.942· 10 ⁻³	6.262· 10 ⁻³	4.628· 10 ⁻³	1.667· 10 ⁻³	1.450· 10 ⁻²	1.225· 10 ⁻¹	2.911	2.000· 10 ¹	1.355· 10 ²	
3-fold SKiiPPACK										
6	2.143· 10 ⁻³	3.818· 10 ⁻³	9.405· 10 ⁻³	2.535· 10 ⁻³	1.790· 10 ⁻²	2.204· 10 ⁻¹	3.343	2.800· 10 ¹	1.123· 10 ²	
10	2.143· 10 ⁻³	3.818· 10 ⁻³	6.683· 10 ⁻³	2.057· 10 ⁻³	1.470· 10 ⁻²	2.204· 10 ⁻¹	3.343	2.367· 10 ¹	1.094· 10 ²	
14	2.143· 10 ⁻³	3.818· 10 ⁻³	5.662· 10 ⁻³	1.878· 10 ⁻³	1.350· 10 ⁻²	2.204· 10 ⁻¹	3.343	2.205· 10 ¹	1.083· 10 ²	

4-fold SKiiPPACK									
6	$8.714 \cdot 10^{-4}$	$2.893 \cdot 10^{-3}$	$7.573 \cdot 10^{-3}$	$1.970 \cdot 10^{-3}$	$1.331 \cdot 10^{-2}$	$9.939 \cdot 10^{-2}$	2.038	$2.700 \cdot 10^1$	$1.462 \cdot 10^2$
10	$8.714 \cdot 10^{-4}$	$2.893 \cdot 10^{-3}$	$4.785 \cdot 10^{-3}$	$2.052 \cdot 10^{-3}$	$1.060 \cdot 10^{-2}$	$9.939 \cdot 10^{-2}$	2.038	$1.868 \cdot 10^1$	$9.085 \cdot 10^1$
14	$8.714 \cdot 10^{-4}$	$2.893 \cdot 10^{-3}$	$3.649 \cdot 10^{-3}$	$2.086 \cdot 10^{-3}$	$9.499 \cdot 10^{-3}$	$9.939 \cdot 10^{-2}$	2.038	$1.529 \cdot 10^1$	$6.830 \cdot 10^1$

Calculation of thermal stacking is basically made the same way as with air cooling.

3.4 Power design

MOSFET, IGBT or SKiiP power circuits are designed in printed circuit board technology, or by means of cables or massive copper or aluminum bars, depending on the currents and voltages to be switched.

Apart from the general specifications to be met, for example with regards to creepage and striking distances or current density, the short switching times within the nano to microsecond range demand a sophisticated power design, which also lives up to the requirements of high-frequencies.

3.4.1 Parasitic inductances and capacitances

To analyse the effects of parasitic inductances and capacitances of converters, it will be sufficient to examine one commutation circuit.

Figure 3.23 shows the commutation circuit of an IGBT-inverter with parasitic elements, consisting of DC-link voltage v_d (corresponds to commutation voltage v_K) and two IGBT switches with driver and inverse diodes. Commutation voltage is impressed by the DC-link capacitance C_d . The impressed current i_L flows out of the commutation circuit.

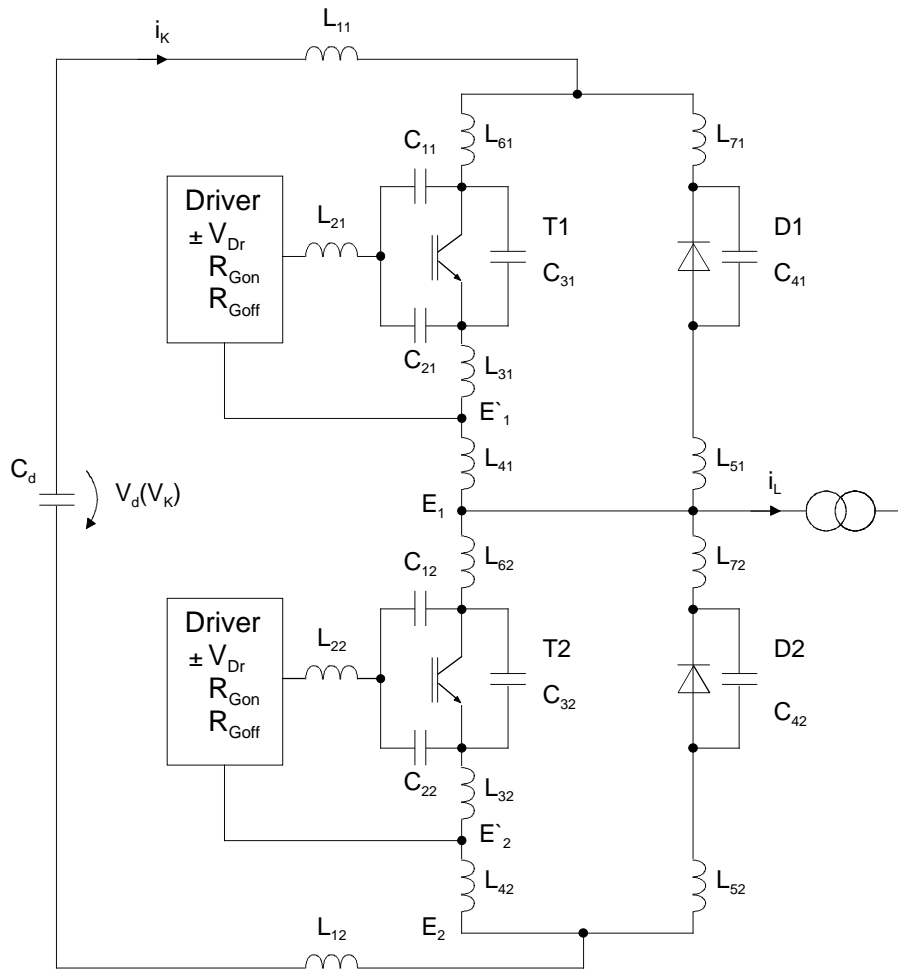


Figure 3.23 Commutation circuit with parasitic elements

The effects of parasitic elements / counter-measures

Total commutation inductance

In the commutation circuit with T1 and D2, the amount of L_{11} , L_{61} , L_{31} , L_{41} , L_{72} , L_{52} and L_{12} is effective as total commutation inductance. In analogy, the amount of L_{11} , L_{71} , L_{51} , L_{62} , L_{32} , L_{42} and L_{12} is effective in the commutation circuit with D1 and T2.

During active turn-on of T1 or T2, respectively, the total commutation inductance becomes effective as turn-on relief, which will reduce turn-on power dissipation in T1 or T2 (see chapter 3.8).

However, during active turn-off of T1 and T2 as well as during reverse-recovery-di/dt of D1 and D2, switching overvoltages are generated in the transistors and diodes due to high di/dt caused by the commutation inductances. This will increase turn-off power dissipation and voltage stress of the power semiconductors.

This effect is especially critical with regards to short-circuits and overload (see chapter 3.6). Moreover, together with parasitic capacitances unwelcome high frequency oscillations may be generated.

Therefore, it is of major importance to minimize inductances in the commutation circuit of hard-switching converters. Except for L_{11} and L_{12} , all inductances are generated in the modules, which may not be influenced by the user. In this respect, it is up to the manufacturers of power

modules, to keep on working on the minimization of internal inductances by improving module assembly technologies (see chapter 1.4).

SEMIKRON datasheets indicate the internal inductances becoming effective at the module output terminals (Example: SKM100GB123D: $L_{CE} = \text{max. } 30 \text{ nH}$).

In the case of single switch modules (1 IGBT/MOSFET + 1 inverse diode), the connection of both modules has to be made as low-inductive as possible in an converter phase.

Low-inductance DC-link power busbars are of special importance. This goes for the connection busbars of the capacitor battery itself as well as for connection of the power modules to the DC-link. In this respect, laminated busbar systems (tightly paralleled plate systems) adapted to the specific inverter layout have gained general acceptance in practice, achieving busbar inductances up to 20...50 nH. Some examples of this are shown in Figure 3.31.

The effects of the remaining inductances $L_{11}+L_{12}$ on the power semiconductors can still be reduced by connecting C-, RC- or RCD-circuits directly to the DC-link terminals of the power modules. In most cases, a simple C-circuit with film capacitors within the range of 0.1...2 μF is connected.

Inductances of emitter or source

The elements L_{31} or L_{32} of the emitter/ source inductances are effective in the power circuit as well as in the driver circuit of the transistors.

Due to the fast di/dt of the transistor current, voltages will be induced which will have the effect of inverse feedback in the driver circuit (emitter/source inverse feedback). This, however, will decelerate the charging process of the gate-emitter-capacitance during turn-on and the discharging of the gate-emitter-capacitance during turn-off, resulting in increased switching times and switching losses.

The inverse feedback effect of the emitter may be utilized for limitation of the collector current di/dt in the case of short-circuits near the modules.

To minimize the inductances L_{31} and L_{32} , power modules are equipped with separate emitter control terminals.

If several BOTTOM driver stages of a converter are supplied by a common operating voltage with negative DC-link reference, the parasitic inductances between the ground connectors of the drivers and the negative potential of the DC-link may cause unwelcome oscillations in the ground loops. This problem can be solved by HF-stabilization of the driver operating voltage near to the output stage or separate supply voltage potentials of the BOTTOM driver stages in high-power inverters.

Inductance L_{21} and L_{22}

Inductances L_{21} or L_{22} , respectively, designate the inductance of the supply line between driver and transistor. Apart from increasing the impedance of the driver circuit, they may cause unwelcome oscillations with the input capacitance of the transistor. This may be remedied by a short, low-inductance connection between driver and transistor.

Capacitances

The capacitances C_{xx} in Figure 3.23 stand for the intrinsic capacitances in the power semiconductors (voltage-dependent, non-linear) and cannot be influenced by the user. They indicate the minimum value of the commutation capacitance C_K and, principally, effect a reduction of power dissipations during turn-off (see chapters 0 and 3.8).

Additional power dissipations are generated during active turn-on due to the recharge process of the commutation capacitances; these have to be considered in many high-frequency MOSFET-applications (...100 kHz...).

C_{11} and C_{12} cause an inverse dv/dt -feedback to the gate (Miller effect, see Figure 3.35).

In combination with the inductances near the switches, the intrinsic component capacitances may cause unwelcome oscillations.

3.4.2 EMI/mains feedbacks

3.4.2.1 Processes in the converter

Processes in a converter system will always produce unwelcome interference due to the switching operation of the power semiconductors on the one hand (Figure 3.24) and welcome energy transmission with the corresponding signal processing on the other hand.

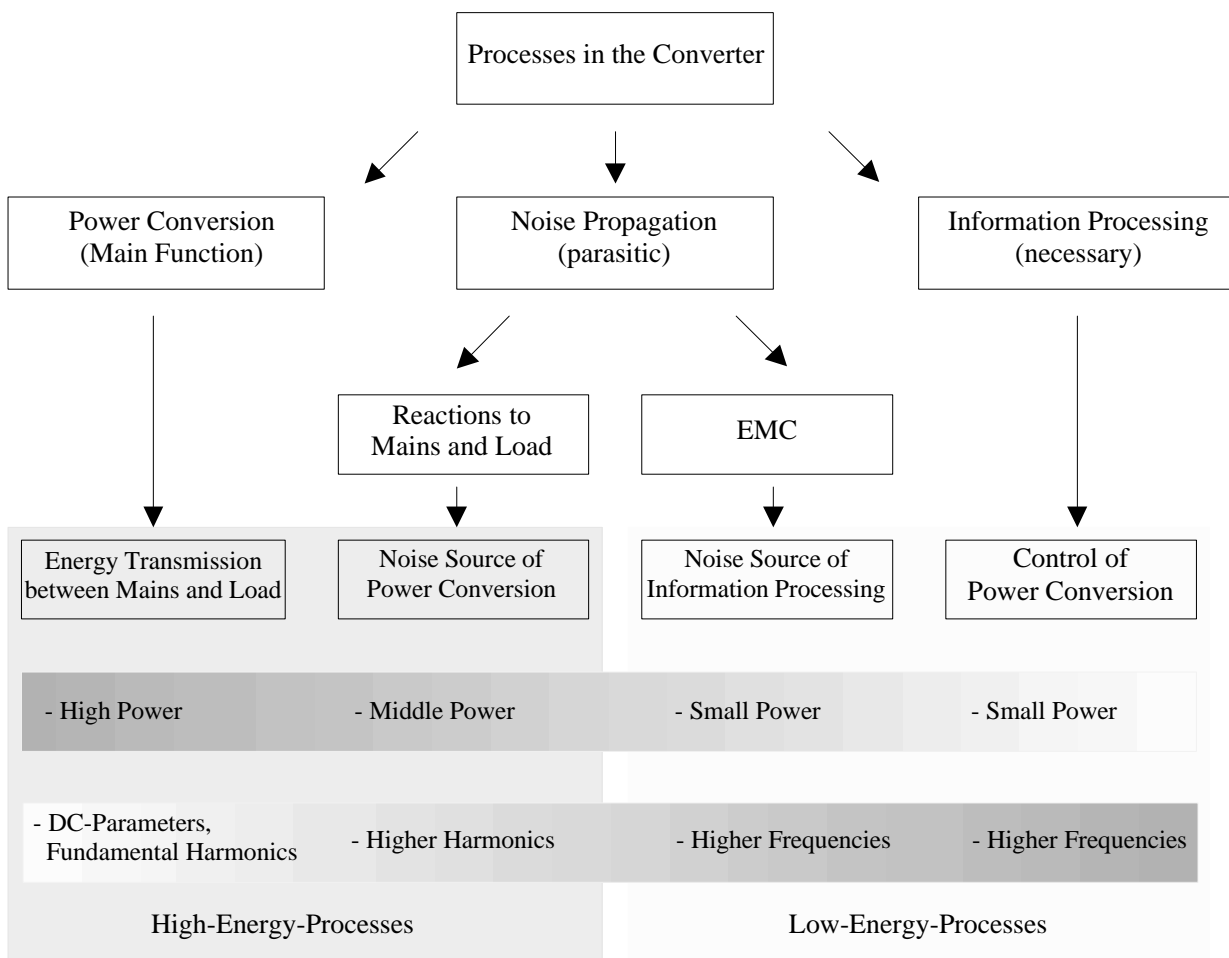


Figure 3.24 Energy processes in converters [299]

These processes can be divided up into high-energy-processes, which may cause interferences in the mains and the load within a frequency range between fundamental frequency and about 10 kHz, and low-energy-processes above 10 kHz up to about 30 MHz, where noise radiation and, consequently, non-conducted current flow will start to be propagated. The frequencies mentioned originate more or less from possible measuring procedures, and not from physical effects. In the low-frequency range, these effects are called converter mains feedbacks, which are

traditionally characterized by discrete harmonic current oscillations up to about 2 kHz. Above 10 kHz these oscillations are called radio interference voltages, which are indicated in dB/ μ V and are designated as interference voltages due to selective measurements. For the interim frequency range, within which modern power semiconductors are switched, the first attempts are currently being made to introduce measuring procedures as well as limit ratings. Discussions on these disturbing side-effects are contradictory, since the same physical processes are described under different aspects. The difference between designations such as zero current, leakage current or asymmetrical interference voltage is only given by various frequency range classifications and by the frequency dependency of all switching parameters. Since this frequency dependency is continuous just as the transition to radio interference, the frequency transition ranges are inevitably very broad.

3.4.2.2 Causes of interference currents

All interference is caused by the switching operation mode of power semiconductors. Causes of interference may be explained by the equivalent commutation circuit in Figure 3.25.

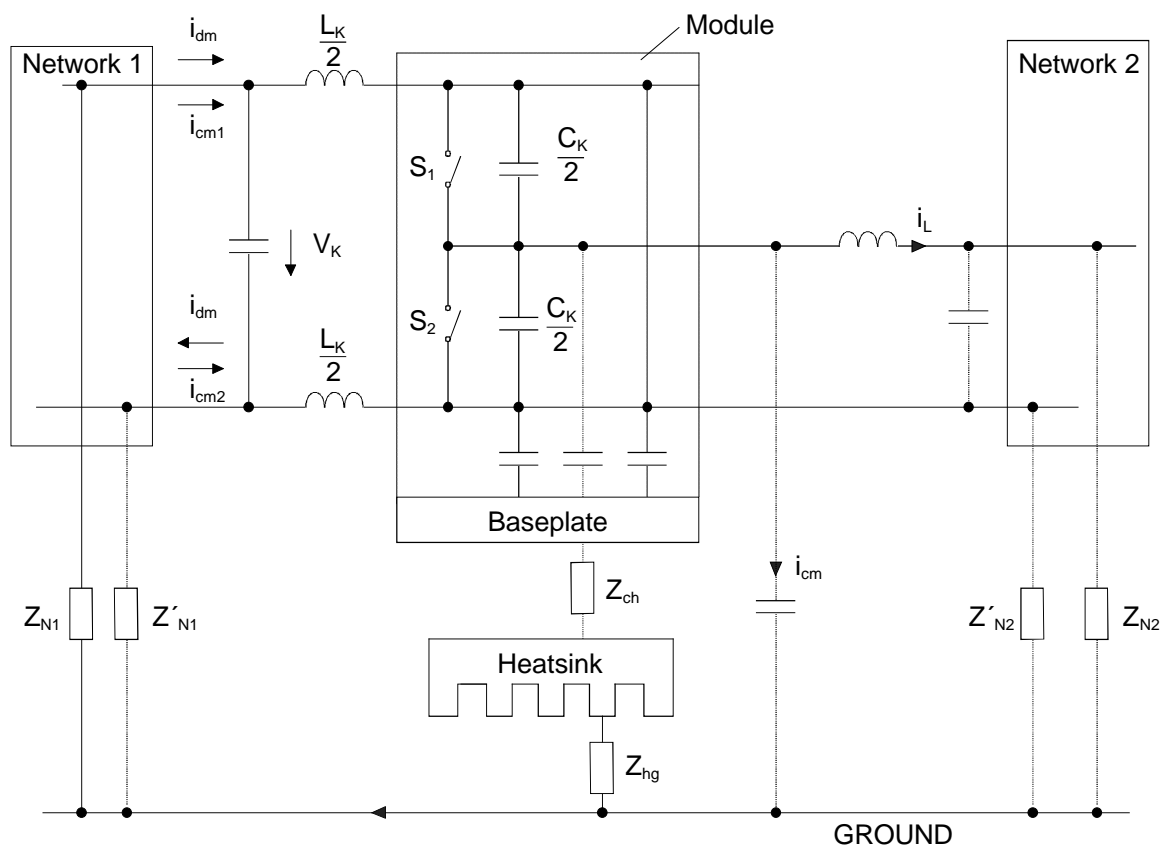


Figure 3.25 Equivalent commutation circuit with noise propagation paths [299]

In the case of *inductive commutation* switch S_1 will switch to the conducting switch S_2 . In a hard switching process ($L_K = L_{Kmin}$, $C_K = C_{Kmin}$) firstly the current will be commutated with a di/dt given by the semiconductor characteristics of switch 1. Commutation is finalized by the reverse-recovery- di/dt of switch 2, which determines voltage commutation and, consequently, dv/dt together with the current-carrying inductance and the effective capacitances C_K . The effective capacitances comprise all capacitances C_Σ which are effective towards the neutral potential. Together with the impedances of the commutation voltage connections to the neutral potential parallel impedances of the commutation capacitances will become effective. At the