600V Converter/Inverter/Brake (CIB) - Module with integrated SOI Gate Driver IC for Medium Power Applications

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Abstract

Intelligent Power Modules (IPM) as fully integrated solution which combine both driving circuitry and power bridges on a single die or at least with implemented IC- based driver replacing conventional hybrid IGBT or MOS drivers are restricted to low power applications (600V/ 1200V, < 30A). With the extension of the current range of the IPMs from 30A up to 100A the medium power market can be served too. A novel approach for medium power IPMs is presented in this paper combining well established CIB-modules based on Semikron's Mini-SKiiP technology with advanced silicon on insulator (SOI) gate driver HVICs in a reliably cost effective and low inductive package and with excellent cooling.

1 Introduction

During some years high voltage integrated circuits (HVIC) tend to substitute conventional hybrid driver solutions in Intelligent Power Modules (IPM) in the 600V and 1200V class for currents of about 20 amps in order to reduce size and costs and to improve reliability. Moreover the use of HVICs allows to integrate more complex functionality without increasing the total costs.

A CIB-IPM solution for medium power applications (600V, 50A) is presented, including a 7-channel SOI gate driver HVIC directly mounted on the DBC substrate of the module.

2 Assembly

The IPM package is based on Semikron's established Mini-SKiiP technology [1]. **Figure 1** shows an assembly example. Its advantages are founded primarily on innovative package without base plate under the DBC substrate and with spring contacts for all main and auxiliary connections between the DBC and the board. The spring contacts are embedded in the plastic housing. The whole system is mounted with the module cap and with only one screw on the heat sink. This leads to an easy assembly with high thermal and power cycling capability, as well as vibration ruggedness. Inside of the package all required power devices, SMDs, sensors and the gate driver HVIC can easily be assembled on the common DBC substrate.

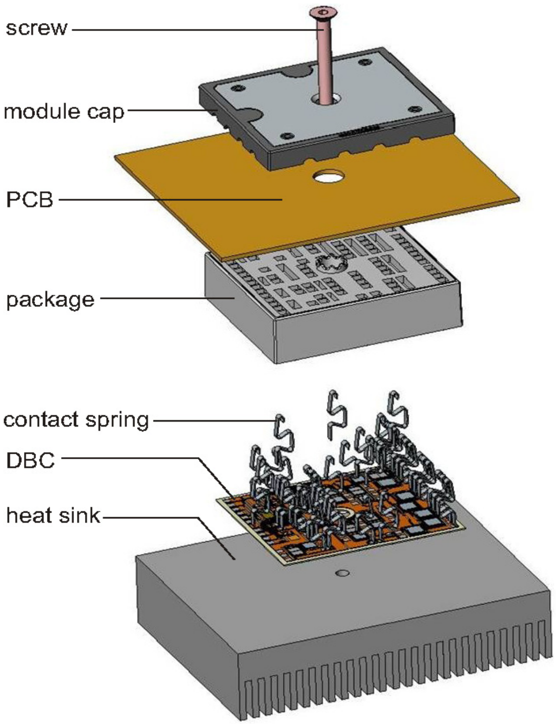

Fig. 1 Mini-SKiiP assembly example

3 Topology and DBC Layout

The circuit topology of the IPM shows **Fig. 2**. It contains the usual power electronic circuit of a CIB module, i.e. a 3-phase converter, a 3-phase inverter consisting of three IGBT half bridges and a brake chopper. The topology was extended by the 7-channel gate driver HVIC, which is able to drive the six IGBTs of the inverter (3 x TOP, 3 x BOT) as well as the IGBT of the brake chopper (BOT). Furthermore a temperature sensor is integrated. **Figure 3** shows the layout of the DBC substrate with all assembled devices. The DBC substrate consists of a thin ceramic plate (0.38mm) and has a copper metallization on both sides (0.2mm). The front side copper layer was structured according to the circuit topology with a minimum pitch of 0.8mm. The power semiconductors and the temperature sensor are back side soldered on the DBC and contacted with thick Al-bond wires on the front side.

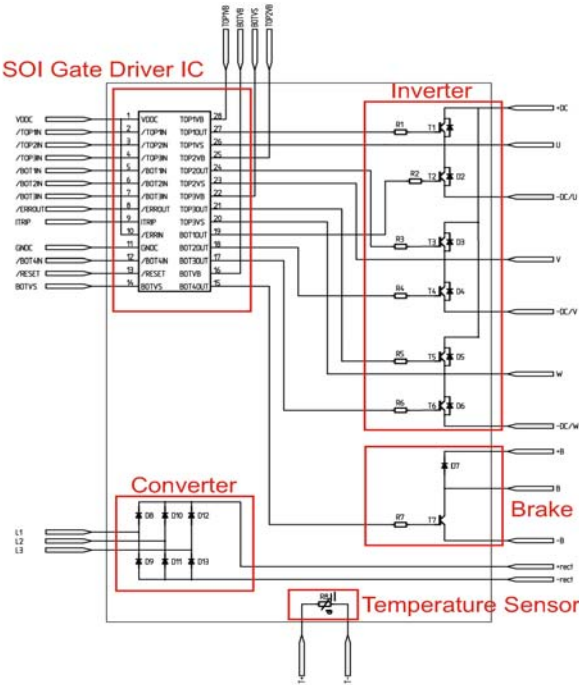

Fig. 2 Block circuit diagram of the new MiniSKiiP-IPM

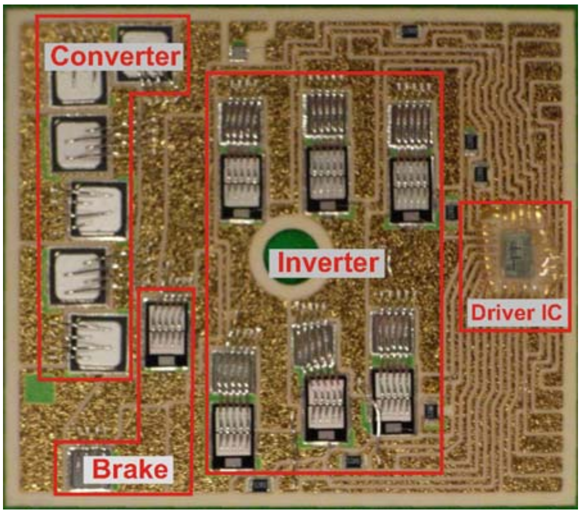

Fig. 3 Photograph of the DBC, size: 57x50mm^2

The gate driver HVIC die and the SMD gate resistors are assembled with conductive glue on the DBC. The contacts between the HVIC-pads and the DBC copper conducting paths are realized by thin (25µm) bond wires (see **Fig. 4**). The routing of the conducting paths on the DBC is very short and compact, so a low inductivity is reached. The HVIC and the thin bond wires can be covered optionally with a special glob top. The DBC substrate and the mounted devices are protected with silicone gel.

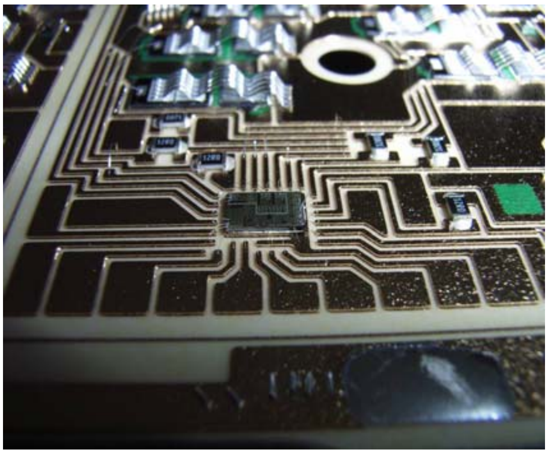

Fig. 4 Assembly of the SOI gate driver HVIC on the DBC substrate

4 600V 7-channel Gate Driver IC

The technological platform for the integrated 7-channel gate driver HVIC is a 600V SOI foundry technology [2] [3] featuring a complete dielectric isolation of every single device showing no appreciable back gate effect. Other important advantages of the chosen SOI technology compared to pn-isolated technologies are considerably smaller leakage currents, an extended operational temperature range (to T_{jmax}=200°C) and a high integration density.

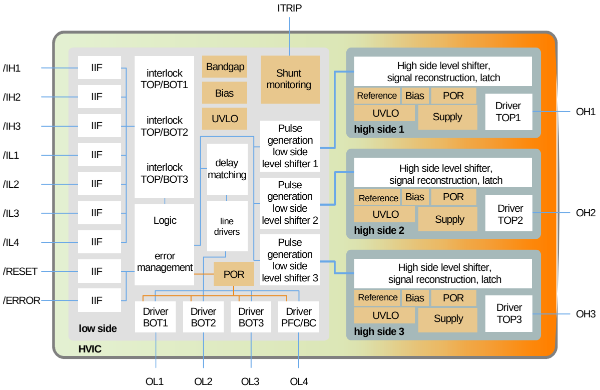

Fig. 5 Block circuit diagram of the 7-channel gate driver HVIC

Figure 5 shows the block circuit diagram of the 7-channel gate driver HVIC. The HVIC processes 3 top (TOP) and 3 bottom (BOT) drive signals with pair-wise hardware interlock and a fourth independent BOT signal which can be used for brake chopper applications or PFC circuits.

An error management circuit is integrated which processes internal error events (under voltage) as well as external error requests applied to the input /IN_ERR and over current events detected by the input ITRIP respectively. In case of an error event all channels are turned off. The bidirectional pin /RESET can send out reset requests for external components, e.g. during the initialization phase after turn on of the supply voltage (power on reset, POR), but can also receive external reset requests and force the HVIC in the initialization state. In this manner a system initialization with other components can be very simply realised with a bus system.

The inputs are compatible to TTL and 3.3V CMOS-logic. The over current input ITRIP generates an error signal if an internal voltage threshold is exceeded (typically 430mV). The driver outputs provide a peak output current of approximately 500mA/ 650mA (source/ sink) at 15V supply voltage and room temperature. Bandgap references for supply voltage monitoring (undervoltage lockout, UVLO) and power on reset (POR) are integrated for the primary side and for the secondary side of each TOP-channel. The supply voltages may vary from 12V to 17V. The typical signal propagation delay between in- and output is about 300ns.

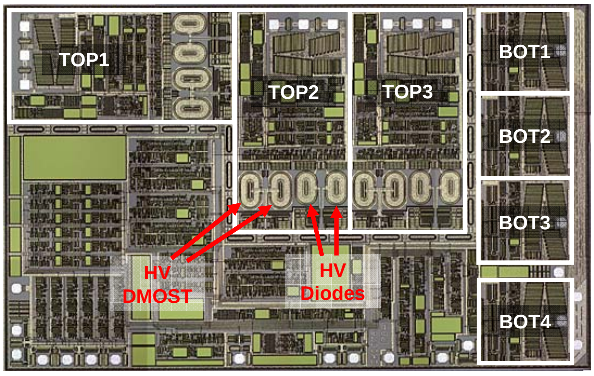

Fig. 6 Chip photograph of the 7-channel gate driver HVIC, size app. 4.9 x 3.1mm^2

Figure 6 shows the chip photograph of the 7-channel gate driver HVIC in the 600V SOI technology. The chip size is app. 15mm^2. The high voltage devices (DMOS transistors, HV diodes) are clearly to recognize in the level shifter circuits of the TOP channels as well as the seven driver stages.

5 Advanced level shifter concept

Even in low current applications and, yet more, in medium and high current applications, where high currents or high dI/dt are switched, positive and negative voltage peaks may occur on parasitic elements in the power plane. These voltage peaks might cause a strong voltage drop between the primary and the secondary side of the gate driver (offset voltage). A negative offset voltage in particular is critical for junction-isolated HVICs [4] [5], commonly allowing only a few volts (typically -5V) below ground potential to prevent latch up [6]. Therefore the design goal for medium power applications is a significant extension of the range of the operational voltage shift between the primary side (control logic) and the secondary side (drivers). This requires an advanced level shifter concept for both the BOT and the TOP channel allowing “bipolar” operation.

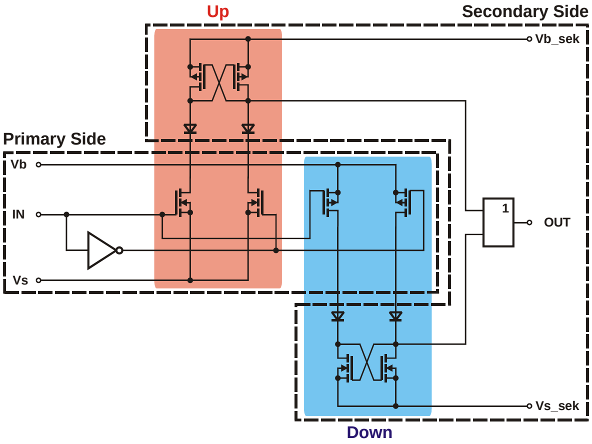

Fig. 7 Circuit principle with up-/down- level shifter for the BOT channel

This specific level shifter concept was realised in our gate driver HVIC [7]. The circuit principle of the BOT channel level shifter is shown in **Fig. 7**. It consists of two independent transmission paths, an up-level shifter and a complementary down-level shifter. The configuration is that of a conventional static CMOS level shifter with additional diodes in each path. Both the up- and the down-level shifters use two cross coupled parallel branches with the function of a latch. Hence there are no cross currents under static voltage conditions. Because of the full dielectric isolation of each device, the circuit itself is latch-up free. For this reason and also that of the weak back gate effect of the used SOI technology every circuit part can carry any desired potential. The maximum allowable offset voltage is only limited by the breakdown voltage of the level shifter transistors.

Depending on the polarity of the offset voltage between the primary side and the secondary side ($V_{offset} = V_{vs\_sek} - V_s$) the up-level shifter ($V_{offset} \geq 0V$) or the down-level shifter ($V_{offset} \leq 0V$) transmits the applied input signal from the primary to the secondary side. The inactive path is blocked by reverse-biased diodes. To reconstruct the signal on the secondary side, a simple logic disjunction can be used.

The circuit principle of the TOP channel level shifter is shown in **Fig. 8**. As in the case of the BOT channel, the level shifter consists of two complementary parts: the high voltage up-level shifter and the low voltage down-level shifter. Because there are no p-MOS devices available with a breakdown voltage extending to 600V, a pulsed signal transmission simply requiring high-voltage n-DMOS transistors and high-voltage diodes, to block the high reverse voltage in the down-level shifter, is used. A pulsed transmission is applied to minimize the cross current and power consumption but requires more complex signal generation and reconstruction in comparison to the BOT channel. The differential transmission with two branches per level shifter, a robust signal processing and reconstruction on the secondary side provide maximum immunity against parasitic coupling from the power plane.

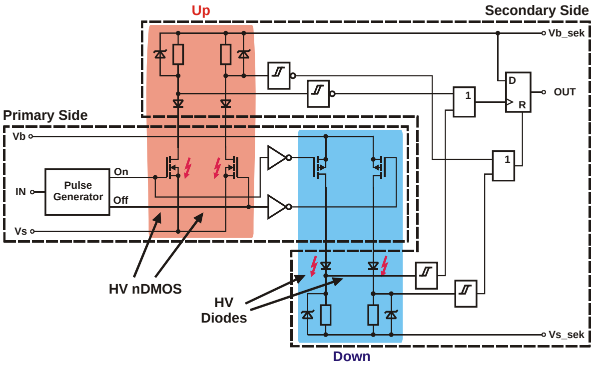

Fig. 8 Circuit principle with up-/down- level shifter for the TOP channel

6 Thermal simulation

To determine the thermal properties of the gate driver-HVIC directly glued on the DBC of an IPM some simulations were made. To carry out the simulations a complete 3d modelling of the HVIC assembly was performed, including the SOI layer structure, the glue layer, the DBC and the heat sink.

Figure 9 shows the temperature distribution in the HVIC for a total power loss of 1W. The main contribution to the total power loss in the HVIC is assumed to originate in the seven drivers stages (uniformly distributed). The heat sink temperature is held on 85°C as a boundary condition. The simulation shows a maximum junction temperature in the hottest driver stage in the lower right corner of $T_{jmax} \approx 89°C$. This shows that the thermal resistance from the junction to the heat sink is very low ($R_{thjh} \approx 4K/W$). This is achieved by the good thermal connection of the HVIC to the heat sink via the DBC substrate.

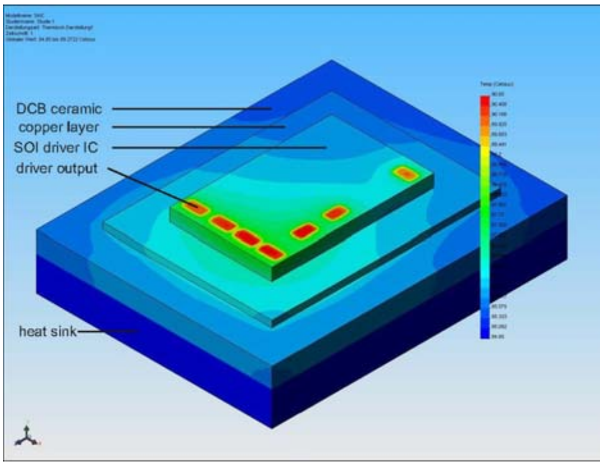

Fig. 9 Thermal simulation of the 7-channel gate driver HVIC on a DBC substrate

7 Measurement results

Some functional tests were made on an IPM assembled with 600V/50A IGBT3 (Trench Fieldstop [8]) and 600V/50A CAL3 freewheeling diodes [1] with focus on the dynamic / switching behaviour.

Figures 10 and **11** show the turn-on and turn-off behaviour of one of the BOT-IGBTs at 400V DC link voltage.

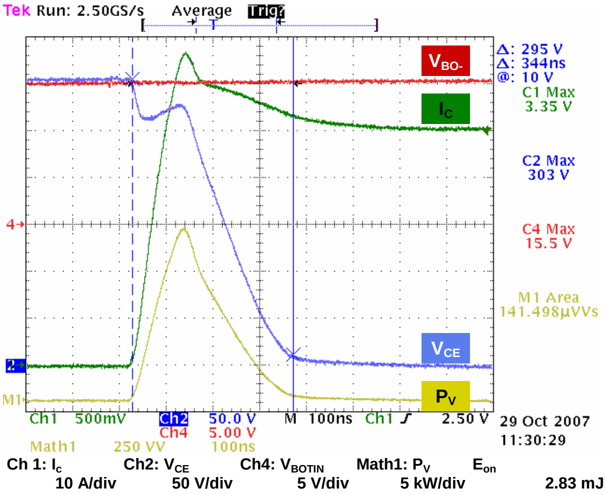

Fig. 10 BOT-IGBT turn-on and switching losses at rated current (50A), V_{DC}=400V, T_{Case} = 27°C

The total switching losses (E_{on}+E_{off}= 4.5 mJ) are somewhat larger than the datasheet values of a comparable Mini-SKiiP (3.2mJ @ 150°C) measured with an external hybrid driver. This is due to the limited driver current of the HVIC (500mA/650mA source/sink). To reduce the switching losses the driver capability might be extended up to 1A prospectively without significant increase of driver chip size. **Figure 12** shows a double pulse measurement of one BOT-IGBT at double the rated current. All the other channels remain unaffected by the large dV/dt and dI/dt transients in this case.

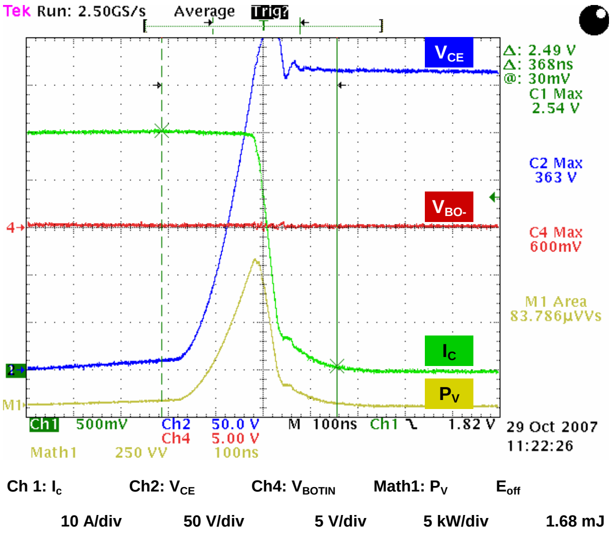

Fig. 11 BOT-IGBT turn-off and switching loss at rated current (50A),V_{DC}=400V, T_{Case}= 27 °C

This indicates a high noise immunity and low crosstalk in the gate driver HVIC. A short circuit measurement (type I, low inductance) is shown in **Fig. 13**. The IGBT is safely turned off at 350A saturation current level while the collector voltage overshoot keeps below 50V ($V_{CE,max}$ = 447V).

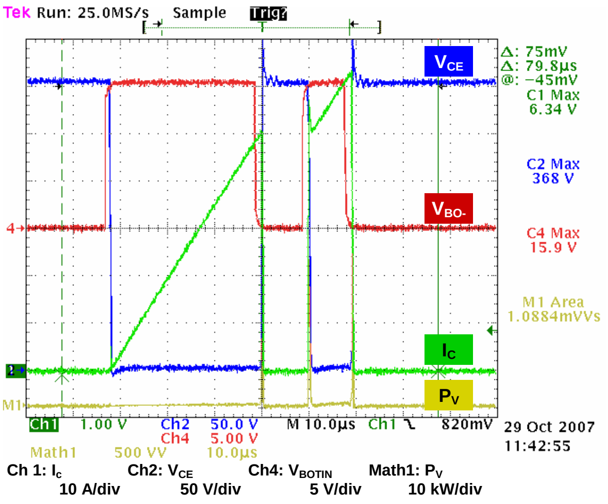

Fig. 12 Double pulse measurement, BOT-channel, switching double the rated current (100A), V_{DC}=300V, T_{Case}= 27 °C

8 Conclusion

A new intelligent power CIP-IPM module for medium and high power applications (600V, 50A) with a very high integration degree and proven assembly was presented. One robust SOI 7-channel gate driver HVIC, using a new level shifter concept allowing to stay fully functional for any applied secondary side reference voltage including negative voltages, is able to drive the IGBTs with high reliability. The excellent cooling of the power semiconductors as well as the driver permits high operating temperatures and leads to a high robustness and a long lifetime.

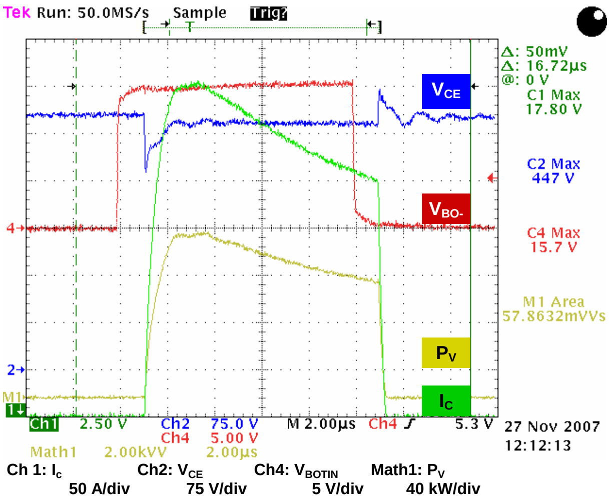

Fig. 13 BOT-IGBT short circuit behaviour (type I, low inductance, V_{DC}=400V, T_{Case}= 27 °C)

9 References

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