Latch-up free 600V SOI Gate Driver IC for Medium Power and High Temperature Applications

M. Roßberg*, R. Herzer*, S. Pawel**
*SEMIKRON Elektronik, **TU Ilmenau
*SEMIKRON Elektronik, Sigmundstrasse 200, 90431 Nuremberg, Germany
**TU Ilmenau, P.O. Box 10 05 65, 98684 Ilmenau, Germany
Tel.: +49 911 6559 182
Fax: +49 911 6559 492.
E-Mail: matthias.rossberg@semikron.com
URL: http://www.semikron.com

Acknowledgements

The authors gratefully acknowledge the help of staff of Philips Semiconductors in Nijmegen (NL), especially that of E. Kluter, A. Strijker and J. Claes.

Keywords

«Design», «Drive», «High voltage IC's», «Power integrated circuit», «Smart Power», «SOI-device», «System integration»

Abstract

The design, functionality and measurements of fully integrated 600V SOI gate drive IC´s are presented. The two-, six- and seven- channel HVIC target different motor drive systems for low power and medium power applications. Dielectric device isolation and the detailed circuit design ensure operation up to a temperature of 200°C. Robust signal processing has been given highest attention at all design stages. A dedicated signal reconstruction topology is presented to provide maximum immunity against parasitic coupling from the power plane. The measurements confirming the safe operation of the ICs are given.

Introduction

IPM solutions for medium power applications (600V, <50A) are aimed at high volume markets, where system costs and geometric size per function are the most relevant parameters. IC-based designs are thus replacing conventional hybrid IGBT and MOS drivers [1] [2] [3] [4].
Due to the high production numbers, fully integrated solutions are feasible which combine both driving circuitry and power bridges on a single die [5]. Widely accepted gate drive ICs rely on conventional junction isolation to achieve 600V blocking voltage and to shield the high side from the offset voltage [6] [7]. Though the market has shown considerable interest in these HV-ICs, the junction isolation entails certain fundamental drawbacks. Negative transient voltages at the driver output can trigger internal parasitic structures, leading to latch-up. The problem can be somewhat alleviated by minority carrier suppression structures [8] [9] [10] but it cannot be resolved completely. Also, increasing pn leakage currents typically limit the operation temperature to 150°C.

600V SOI Technology

A high voltage SOI platform, on the other hand, can provide complete latch-up immunity since all active devices are dielectrically insulated. This enables the operational temperature range to be considerably extended.

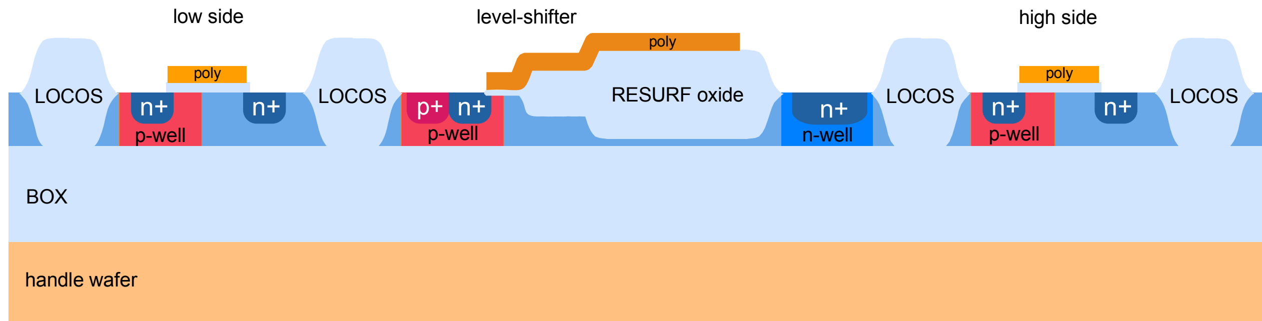


Fig. 1: Schematic cross section of the High Voltage-SOI-IC [11] [12]

The chips were made with a 600V SOI foundry process [11] [12]. Fig.1 shows the schematic cross section of the 600V SOI technology. The CMOS- circuits of the *low side* and the *high side* are based on quasi-bulk-transistors in fully dielectric isolated silicon islands. The active silicon is thick enough to prevent punch-through of the back side space charge region to the top side devices. The theoretical upper limit for the necessary active silicon layer thickness is calculated as shown in Fig. 2 for a temperature range between -23°C and 227 °C.

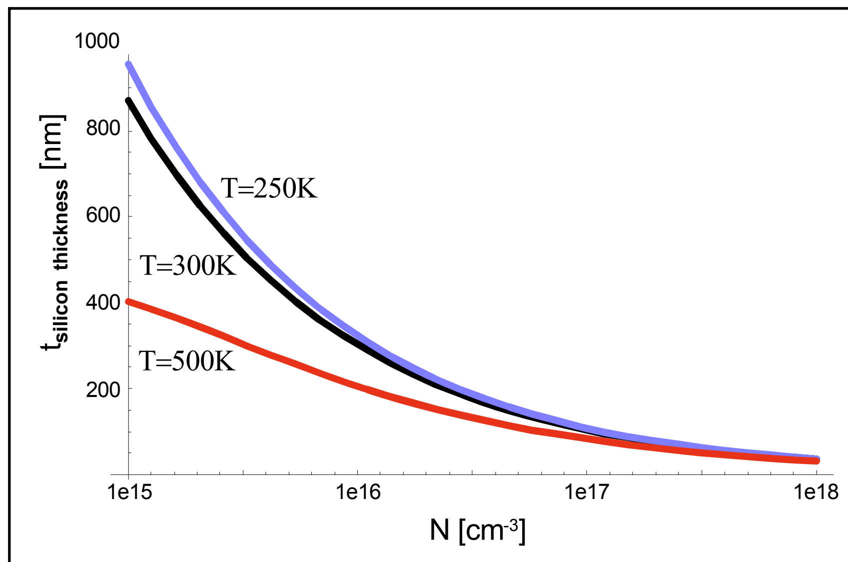
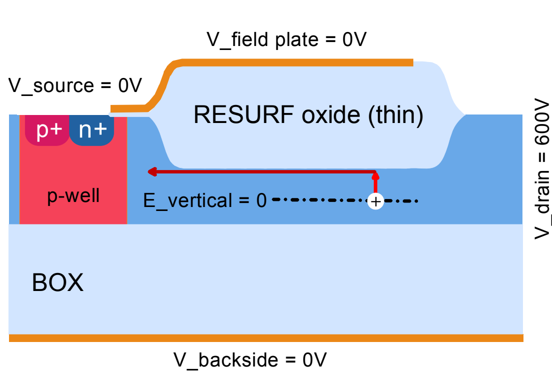


Fig. 2: Minimum silicon top layer thickness preventing the influence of the back gate (1d- calculation)

The keys to the high breakdown voltages are the thick buried oxide layer and the selective layer thinning in the drift region of the high voltage devices [13] [14]. Figs. 3 and 4 illustrate the operation principle. While the lateral ionization paths are the same in both cases, the carrier multiplication due to vertical field components is drastically reduced in Fig.4 because of the reduced vertical avalanche path length.



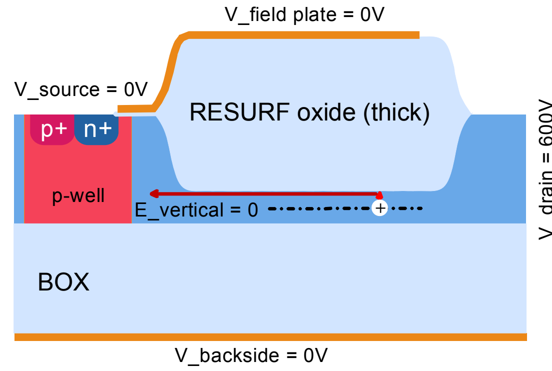


Fig. 3: Vertical and lateral avalanche path in thick active silicon

Fig. 4: Vertical and lateral avalanche path in thin active silicon

In order to determine the breakdown voltage limit of the structure in Figs. 3 and 4, the worst case avalanche paths along the vertical and lateral device dimensions can be calculated. This is not an exact solution because of the two dimensional nature of the problem. For integrated level shifter transistors such as being used in gate drive ICs, the lateral field components can be adjusted by choosing the appropriate drift zone length. This is not a design constraint, since the current levels of the level-shifter are low. Therefore, the vertical component limits the maximum breakdown voltage. The well-known Chynoweth relation [15] and its parameterization according to van Overstraeten and de Man [16] are commonly employed to model avalanche multiplication in drift zones of power devices. However, at high fields and especially over short path lengths, more physically motivated models such as the ones after Okuto/Crowell [17] [18] or Lackner [19] give more consistent predictions. It should be noted, that most analytical formulations of the problem are based on the polynomic Fulop model [20], which must not be used in this range of field strengths. Fig. 5 gives a comparison of the maximally sustainable fields according to different models. The diagram refers to a one-dimensional vertical field with triangular shape as found in the structures of Figs. 3 and 4. The field drops from its peak value E_{MAX} at the silicon/oxide interface to zero towards the middle of the active layer. Thus, the ionization path length is half the active layer thickness.

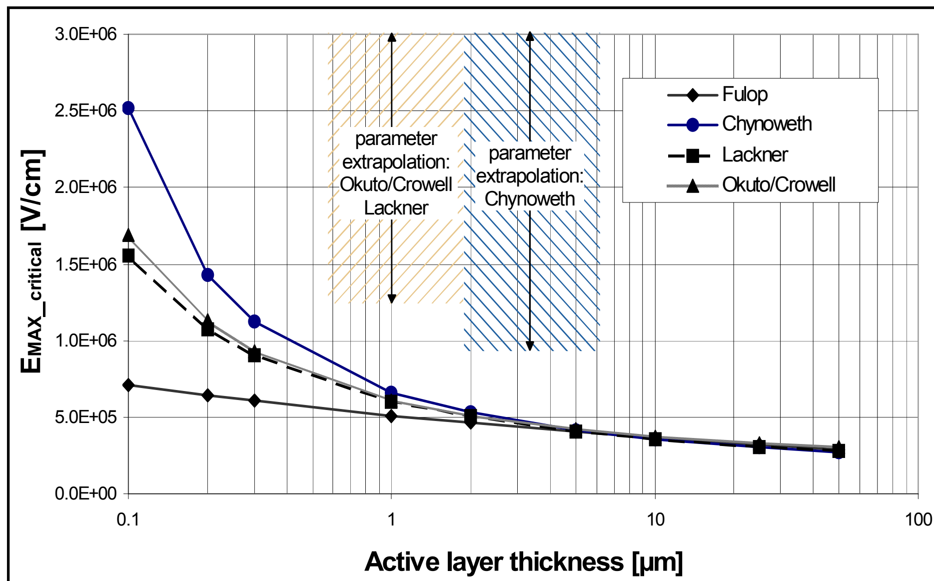


Fig.5: Comparison of critical peak field values

The value $E_{MAX_critical}$ denotes the peak field value where the avalanche integral approaches 1. The models after Okuto / Crowell and Lackner better represent device physics. The mutual consistency of their results supports the assumption, that these models should replace the Chynoweth model for the given case.

System and HVIC design

Fig. 6 shows a block circuit diagram of a three- phase power conversion system. The topological blocks to be integrated into a gate driver HVIC are marked (orange). Depending on the different applications half-bridge- and six-pack-driver ICs are also possible, as well as the integration of additional blocks such as bootstrap-diodes, charge pumps for power supply and V_{CE} detection diodes.
The block circuit diagram for a seven-channel gate driver-IC is given in Fig. 7. Input interfaces (IIF) implement logic thresholds for direct connection to 5V or 3.3V micro controllers. An interlock time is usually implemented in the external drive controller pattern and the user can activate a hardware interlock in the gate driver. Both methods minimize cross-currents in the external power bridge.

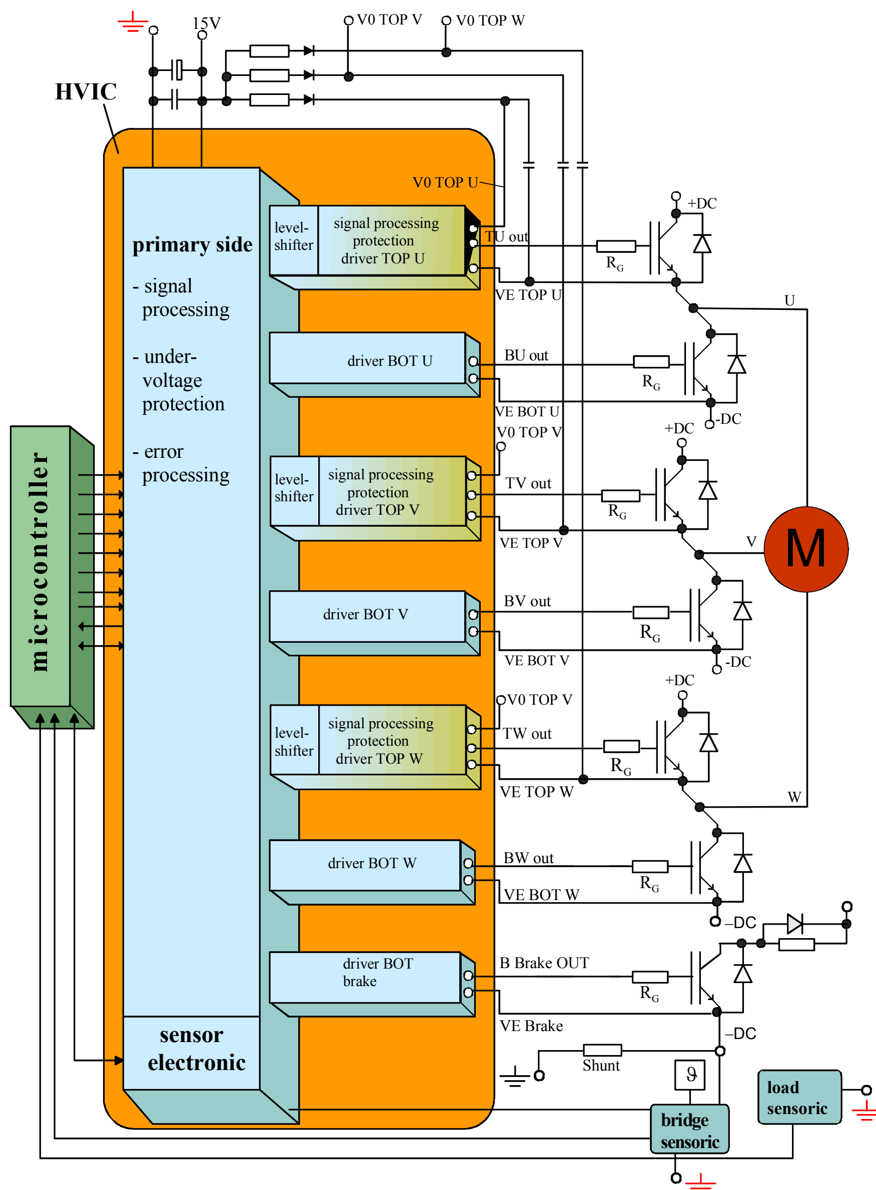


Fig. 6: Power conversion system showing gate driver HVIC integration area

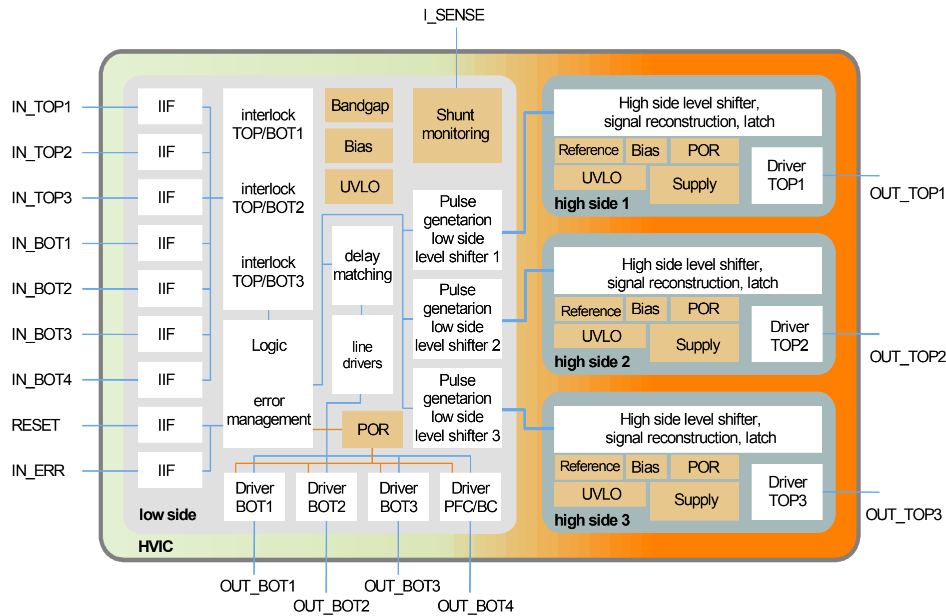


Fig. 7: Block circuit diagram: seven-pack gate drive HVIC

The logic and error management generate the appropriate internal signals. These take into account under voltage lockout (UVLO) as derived from a bandgap-stabilized reference, and external analog sensor signals such as shunt current or temperature monitoring.
The branch delay times of the six main channels TOP/BOT1-3 are delay-matched to ensure synchronized switching. A 7th channel is implemented at the low side to support power factor correction schemes or to be used as a brake chopper.
Three 600V level-shifters transfer the signals to the fully isolated high sides, where the differential transmission signals are filtered and reconstructed. The signals are driven at the chip output by a CMOS stage of the 500mA sink / 250mA source type. The driver operates at 15V. High side supply is implemented by a bootstrap circuit with integrated HV diodes. Fig. 8 is a photograph of an evaluation version carrying additional test pins.

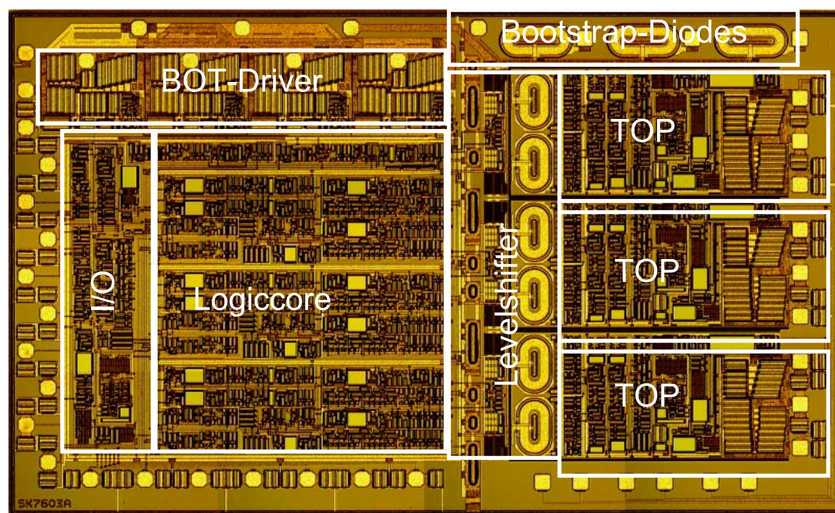


Fig. 8: Chip photograph of the seven-pack gate drive HVIC with bootstrap diodes (chip size approximately $12mm^2$)

Level-shifter design

The single most important internal function of the gate driver IC is to transmit signals from the controlling low side to the three high sides. The signal reconstruction scheme at the high side, in particular, where the transmitted raw pulses are interpreted and converted into valid control patterns, is of fundamental importance. The reconstruction scheme has to separate signals from any voltage or current disturbances which couple back into the IC from the electromagnetically polluted system environment. The raw signal transmission uses two conventional cascode switch configurations as shown in Fig. 9. The 600V device isolates the low side from the high side. As soon as the transistor M_1 opens, a cross-current (I) flows from the high side supply (Vdd_hs) to the low side ground (gnd_ls). The current is limited in M_1 by source feedback over R_{lim}. The voltage drop across R_hs is the high side raw signal (V_{OUT}).
A differential scheme is necessary because of common mode currents flowing through the cell during every dv/dt event between low side and high side. These events are caused by normal switching on or off of the respective channel or by parasitic coupling between channels. The signal reconstruction which has been developed and shown in Fig. 10 relies on individual recognition and processing of the two raw signals rather than a conventional conversion, from differential to single-ended, using latching stages.
The high robustness obtained for the level-shifter is due to the combination of three factors: wide signal swings with interface hysteresis; simple, yet effective logic filtering of common mode signals; and short pulse suppression. This result has been proven by experimental results presented later on. The signal POR (power on reset) in Fig. 10 ensures defined power-up of the latch that is storing the drive information.

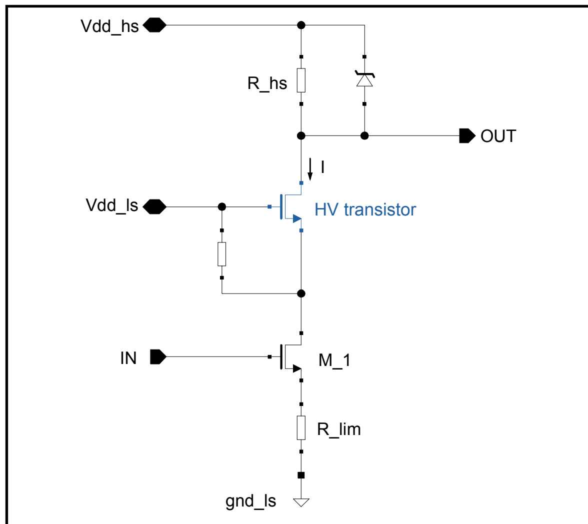


Fig. 9: Level-shifter cell (twice per channel for differential transmission)

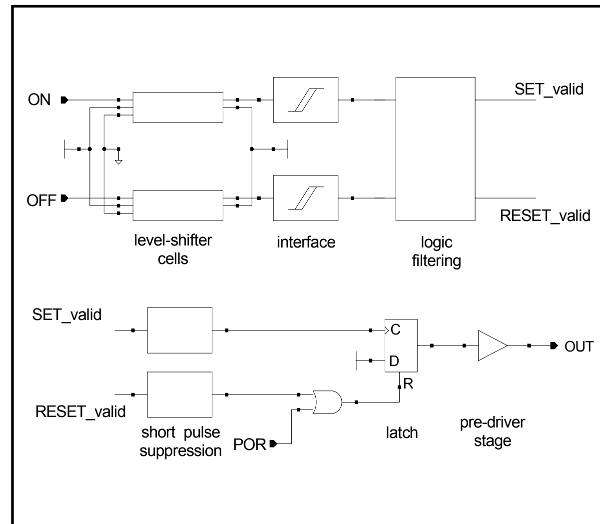


Fig. 10: Signal reconstruction topology

Measurements

All high voltage measurements were taken with the gate drive ICs operating on a SEMIKRON MiniSKiiP II- module (six-pack, 600V / 10A Trench IGBT with CAL free-wheeling diode). The module outputs are connected to individual resistive-inductive loads. Fig. 11 shows a photograph of the measurement setup.

A. Normal operation

The switching of one channel pair at active hardware interlock is demonstrated in Fig 12. The TOP switch turns on (OUT_{TOP}) at a valid on-signal (IN_{TOP}) and turns off if an on-signal occurs at IN_{BOT} to avoid a short circuit in the halfbridge (defined safety regime).

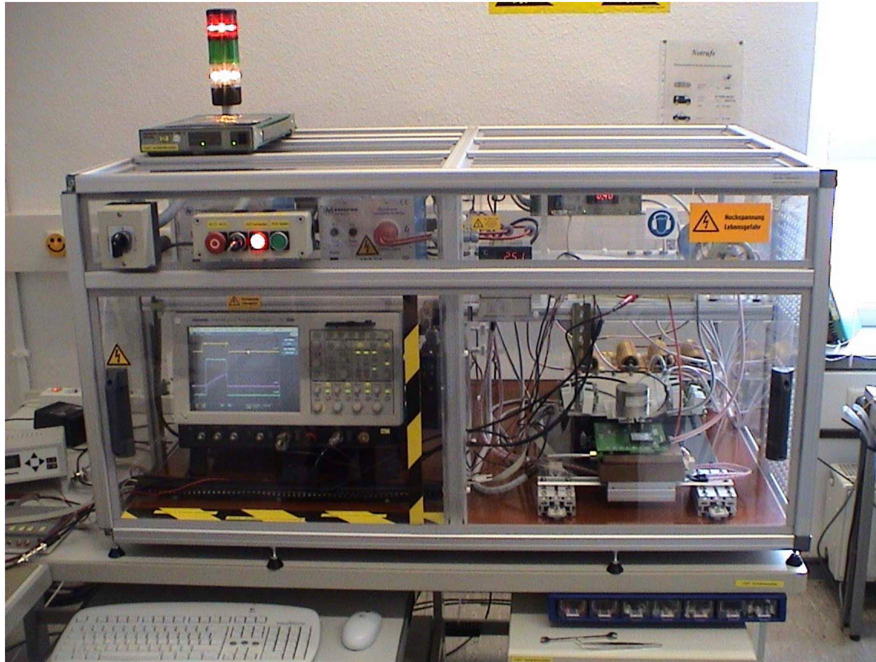
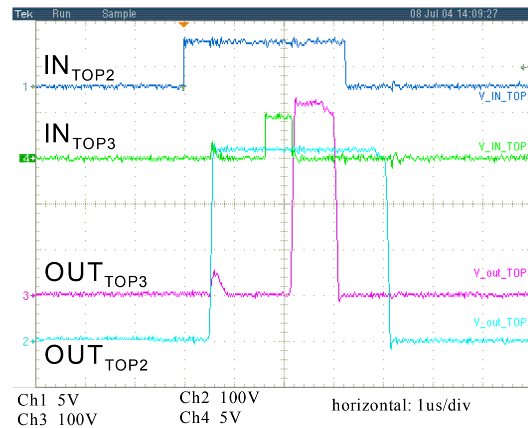


Fig. 11: High voltage measurement setup

Fig.13 shows simultaneous operation of two TOP channels at 400V DC link voltage. No signal interference was observed between the neighboring high sides of the gate driver. The channels can have arbitrary mutual timing.

Fig.14 illustrates the running time of different BOT channels for the same input signal. The differences between BOT 1…3 are maximal 30ns. The total running time is matched to the delay time of the corresponding TOP channel signal paths (TOP 1…3). The channel BOT 4 (brake chopper) runs independently of the other channels without delay time matching.

Fig. 12: Switching of one channel pair (TOP1/ BOT1) at active hardware interlock



Ch1 5V Ch2 100V horizontal: 1us/div
Ch3 100V Ch4 5V

Fig. 13: Independent switching of two TOP channels at 400V DC link voltage

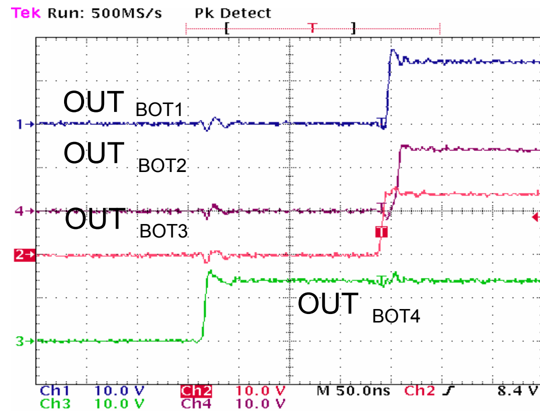


Fig. 14: Running time of different BOT channels

B. Robustness of operation

Several potentially hazardous situations that exceed the limits of regular operation have been tested. As a worst case scenario Fig.15 shows an intentionally strong coupling of electromagnetic fields induced by the load inductivity to the input signal of 3.3V. Additionally the load current oscillations were amplified by the stray inductivities of the measuring setup. Although the noise amplitude is twice as much as the input signal the chip internal filtering and signal reconstruction doesn't interpret it as valid signals.

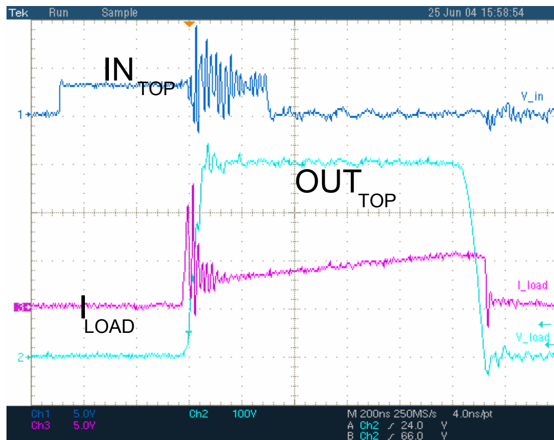


Fig. 15: Double pulse measurement with increased noise coupling on 3.3V input signal (2nd pulse shown)

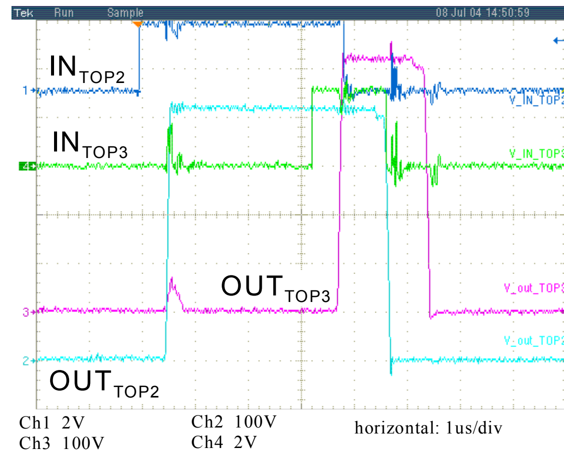


Fig. 16: Safe 3.3V signal recognition at V_{DC}=500V

Fig. 16 presents measurements at increased DC link voltage of 500V. The most critical timing is shown where a phase of high dv/dt at the output of channel TOP3 coincides with a signal transition at the input of channel TOP2. Even at 3.3V input level the internal signal filtering safely recognizes the transition.
Another measurement is shown in Fig. 17 of the IGBT turning on into a hard short circuit and generating harsh current and voltage transients. Internal shunt monitoring produces a reaction as soon as the current rises above the short circuit threshold. A local error signal I_ERR tracks the fault. The global error signal ERR_OUT is generated and sent back to the micro-controller and the IGBTs are turned off.

C. High temperature operation

While the IC has been standard- tested at ambient temperatures between -40°C and 105°C, additional measurements have been taken at core temperatures up to 193°C (Fig. 18). This correlates with driver stage temperatures above 200°C. All outputs were switched at a capacitive load of 2nF each. The core temperature was measured using an internal temperature calibrated diode. The IC retained full functionality at all temperatures.

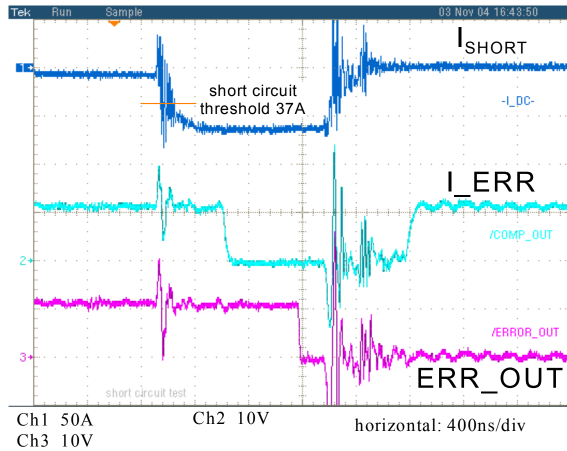


Fig. 17: Short circuit management (hard short circuit)

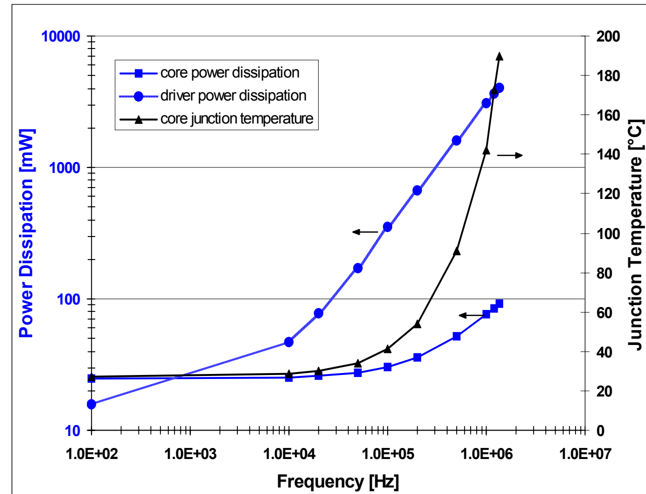


Fig.18: Power consumption and core temperature measurement (capacitive load)

Defining the maximum temperature for continuous operation requires that the lifetime of the on-chip metal interconnects must be taken into account. For the measurement given in Fig. 18, the employed TQFP package was limiting the temperature range. Even at switching frequencies above 1MHz, the IC core dissipates less than 100mW. Thus, high operation robustness has been achieved with low current consumption.

Additional functionality

In addition to the characterized seven-pack driver IC other driver configurations like half-bridge and six-pack driver ICs are possible. Driver-ICs with more powerful output stages and isolated BOT stages are to the best advantage for higher power application. On the other side functionality enhancements, which increase the reliability, availability, safety and ruggedness of the system are preferable. This might incorporate for instance circuit elements for Vce-monitoring of short circuit conditions of each IGBT, temperature and power supply monitoring, status and failure transfer from high to low side and a stable, independent power supply for the high voltage side.

Such another version, a half-bridge driver IC with integrated charge pump for the high side power supply of the core, is shown in Fig. 19. The additional charge pump is using an internal 600V capacitor to provide high side standby power to allow unrestricted switching with no need to recharge the bootstrap capacitor in fixed cycles (independence from PWM signal). Fig. 20 shows the measurements of an integrated test circuit. The transferred current as well as the power efficiency factor vs. the high side supply voltage for different clock frequencies is shown. The power capability of the charge pump is adequate to supply the high side core power consumption (< 100µA) and to drive small capacitive loads (gate capacitance of power switch) at low frequencies. For higher frequencies and/or loads a combination of charge pump and bootstrap power supply is essential.

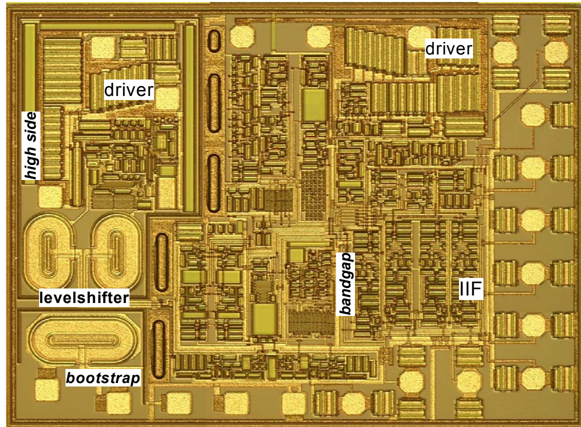


Fig. 19: Chip photograph of a 600V halfbridge gate driver IC (Imax_out= 530mA sink/ 270mA source)

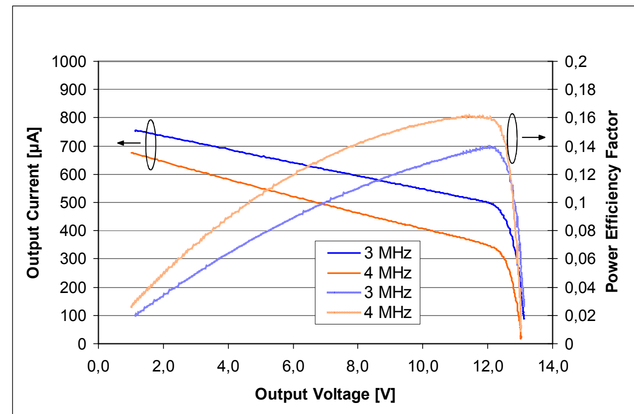


Fig. 20: Measurements of 600V charge pump for continuous high side floating supply (12V version)

Conclusion

High voltage SOI technologies are available that allow monolithic integration of gate drive HVIC for 600V systems. In determining the maximum sustainable voltage, advanced avalanche models are to be preferred over the common Chynoweth relation. Specific work on signal integrity and robustness against coupling from the power environment has led to safe HVIC operation under all conditions tested: low voltage input, high output dv/dt, short circuit and driver stage temperatures higher than 200°C. Functionality enhancements like integrated charge pump to allow unrestricted switching are presented.

References

[1] Data sheet, SPM™ DIP-SPM, Fairchild Semiconductor, 2003
[2] Data sheet, IRAMS06UP60A, International Rectifier, 2003
[3] Data sheet, DIP-IPM, Mitsubishi Electric, 2002
[4] Sung-il Yong, Bum-Seok Suh et al., Power Systems Design Europe, Issue September 2004, pp. 12-17
[5] H. Akiyama et al., Proceedings ISPSD 2004, pp. 375-378
[6] Toshio Takahashi, Proceedings CIPS 2000, pp. 73-81
[7] Data sheet, L6384, STMicroelectronics, 2000
[8] S. Gupta et al., IEEE Electron Device Letters, Vol. 22, No. 12, 2001
[9] J.P. Laine, O. Gonnard, G. Charitat et al., Proc. ISPSD 2002, pp. 273-276
[10] V. Parthasarathy, V. Khemka, et al., Proc. ISPSD 2004, pp. 427-430
[11] T. Letavic, E. Arnold, M. Simpson et al., Proc. ISPSD 1997, pp. 49-52
[12] T. Letavic, M. Simpson, E. Arnold et al., Proc ISPSD 1999, pp. 325-328
[13] S. Merchant et al., Proceedings ISPSD 1991, pp. 31-34
[14] S. Merchant et al., Proceedings ISPSD 1993, pp. 124 – 128
[15] A.G. Chynoweth, Phys. Rev., Vol. 109, Number 5, pp. 1537-1540, 1958
[16] R. van Overstraeten et al., Solid State Elec., Vol. 13, pp. 583 – 608, 1970
[17] Y. Okuto, C. R. Crowell, Phys. Rev. B., 6(8), pp. 3076 – 3081, 1972
[18] Y. Okuto, C. R. Crowell, Phys. Rev. B.,10(10), pp. 4284 – 4296, 1974
[19] T. Lackner, Solid-State Electronics, Vol. 34, pp. 33 – 42, 1991
[20] W. Fulop, Solid-State Electronics, Vol. 10, pp. 39 – 43, 1967