

Electrical and thermal optimization of an automotive power module family

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Abstract: The design of power modules for hybrid cars, trucks and off road vehicles requires unique ways of power electronics integration and packaging. The conflicting requirements of highest power density, high ambient temperatures, reliability and lowest cost can only be fulfilled by a careful selection of IGBT and Diode chips, innovative packaging technologies and a consequent optimization of all thermal and electrical device parameters.

Keywords: power modules, IGBT, hybrid car, packaging

1. SKiM® Power Module Family

The new family of SKiM® (Semikron Integrated Module) power modules is the next generation of ultra compact pressure contact modules without base plate. Instead of soldering the DBC (direct bonded copper) substrate to a baseplate it is pressed directly to the heatsink. Multiple pressure contacts next to each chip are used, keeping the DBC flat and no bimetal effect known from modules with base plates is disturbing the thermal performance. The elimination of a baseplate assures high temperature cycling capability (no solder fatigue caused by CTE mismatch) and a low thermal resistance.

Figure 1 shows the package outline and Figure 2 the cross section of the device with the pressure contact system and the auxiliary spring contacts.

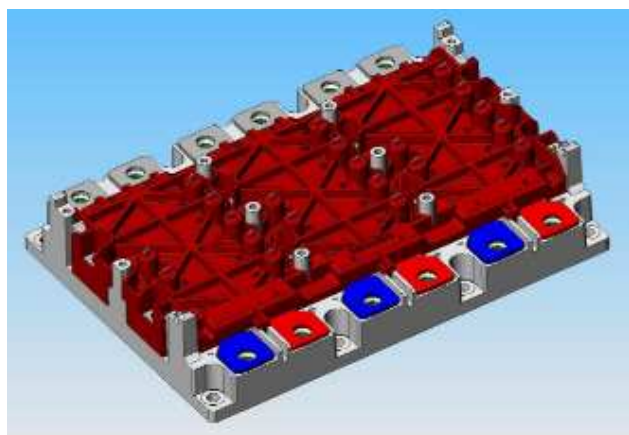


Fig. 1 Package outline SKiM63

The electrical circuit is a Sixpack module with 3 individual half bridge sections. Each half bridge

section has its own DC terminals and an integrated NTC temperature sensor. The auxiliary contacts to control the IGBT's are made with spring contacts. The gate drive PCB does not have to be soldered to the module. Instead the driver is screwed on top of the module assuring a high temperature cycling and vibration-prove reliable spring contact.

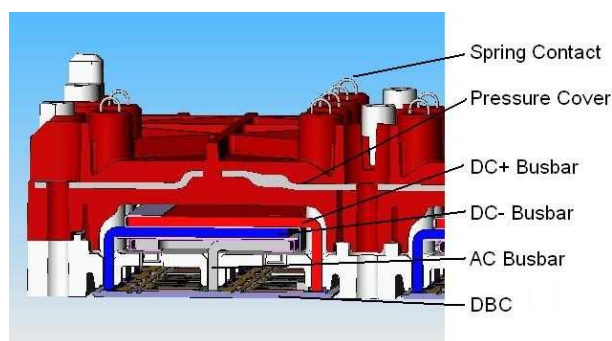


Fig. 2 Cross section of SKiM Module

The devices are expected to be used in a power range between 30kW and 150kW, depending on cooling and operation conditions. Table 1 gives an example of the possible inverter output currents with the SKiM modules.

	SKiM 63	SKiM 93	
$R_{thjs\ IGBT}$	0,14	0,095	K/W
$R_{thjs\ Diode}$	0,27	0,18	K/W
$I_C\ nom.,\ 600V$	600	900	A
$I_C\ nom.,\ 1200V$	300	450	A
$I_{RMS,\ 600V}^{1)}$	280	410	A
$I_{RMS,\ 1200V}^{2)}$	165	250	A

¹⁾ with $U_{DC}=400V$, $U_N=230V$, $\cos\phi=0,8$, $f_{sw}=10kHz$, $T_{jmax}=150^\circ C$, $T_a=80^\circ C$, $R_{th\ cooler} = 8K/kW$ (SKiM93); 12K/kW (SKiM63)

²⁾ with $U_{DC}=750V$, $U_N=400V$, $\cos\phi=0,8$, $f_{sw}=8kHz$, $T_{jmax}=150^\circ C$, $T_a=80^\circ C$, $R_{th\ cooler} = 8K/kW$ (SKiM93); 12K/kW (SKiM63)

Table 1: Main module parameters

2 Busbar Design

A unique feature is the laminated internal busbar structure (Fig. 3). It was designed and optimized to fulfill multiple functions within the module:

- low inductive, low resistive symmetrical connection between main terminals and

chips for good current sharing between the parallel chips

- high current capability for high power inverter design
- providing pressure close to each chip for low thermal resistance

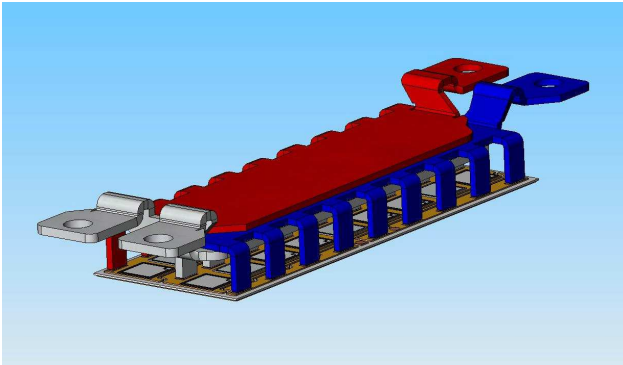


Fig. 3 Laminated busbar sandwich with multiple pressure contacts to the DBC

The DC positive, negative and the AC busbar are made of stamped and folded copper sheets. The busbar sandwich construction is pressed to the DBC substrate with multiple pressure contacts next to each chip. High contact forces assuring a low contact resistance, no additional solder joints are necessary.

2.1 Low inductive design

The sandwich structure with parallel connections to each individual chip assures an ultra low internal inductance. The inductance L_{CE} between a screw of a DC terminal and an AC Terminal is below 10nH with a total inductance from plus to minus DC of less than 20nH.

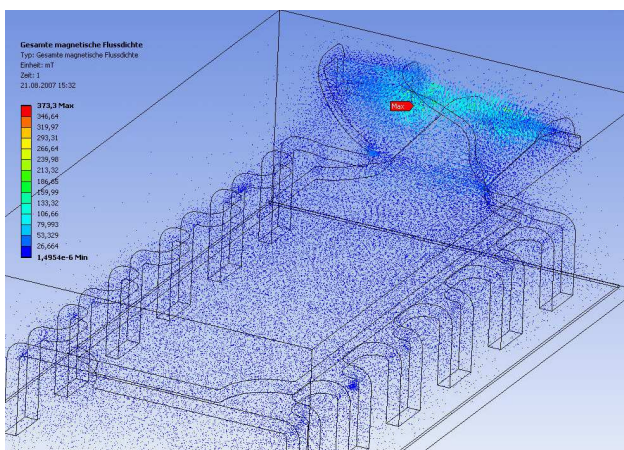


Fig. 4 Simulation of the magnetic field strength and the inductance of the SKiM terminals

FEM Simulations have shown that the main part of it is caused by the distance between the end parts of

+/-DC terminals, where the sandwich can not be realized anymore (see Figure 4). With an optimization at this point a reduction of 30% (-10nH) could be achieved. A further improvement is hardly possible, because of other restriction like creepage and clearance distances. Significant lower values are only possible with multiple parallel connections to the DC link, which were realized in the Semikron AIPM module [1].

The benefit for the user is the low internal voltage overshoot at high di/dt, which allows an operation at high DC link voltage levels and a safe turn-off even under short circuit conditions. Clean switching waveforms without any oscillations leading to low switching losses and low EMI. Furthermore the synchronous switching assures nearly identical switching losses in all chips.

Important for a high utilization of the device blocking voltage is also that nearly no difference in the voltage peak between the different chip positions could be measured (Fig. 5). The internal peak voltage at a turn-off with $I_C=400A$, $V_{CC}=700V$ and $di/dt=6600A/\mu s$ was measured between 929V and 936V at chip positions close to DC terminal, in middle position and close to AC terminal. This is an indication for the symmetric layout with a equal impedance of the current path for each single IGBT chip.

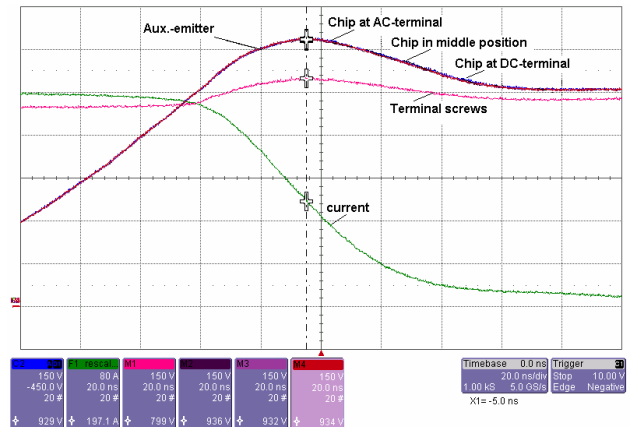


Fig. 5 IGBT turn-off, Voltage measurement at DC-terminal screws and at different Chip positions

2.2 Current capability

Improvements in latest power semiconductor generations allow higher and higher power density within small package designs. The nominal chip current of a 600V SKiM93 is after all 900A. Beside of the device cooling reaches the main terminal current capability of existing solutions its limits. A new busbar system design had also to guarantee a higher current capability, which was realized with wide and thick copper sheets. The resistance of the pure copper part is only between 50 and 60 $\mu\Omega$, the total resistance $r_{CC'-ee'}$ including contact resistances is

about $300\mu\Omega$. The flat module design and the high number of short contacts to the cooling surface of the DBC remove the power dissipation easily into the heatsink.

The AC terminal in inverter application has to carry a $\sqrt{2}$ higher current than the DC-terminals. This was considered with the lower position in the sandwich system with the best cooling. The achievable continuous rms current can be 600A for the AC terminal and 425A for the DC terminals under the condition that the heatsink temperature is 70°C and the temperature at the screw contacts of the terminals does not exceed 115°C .

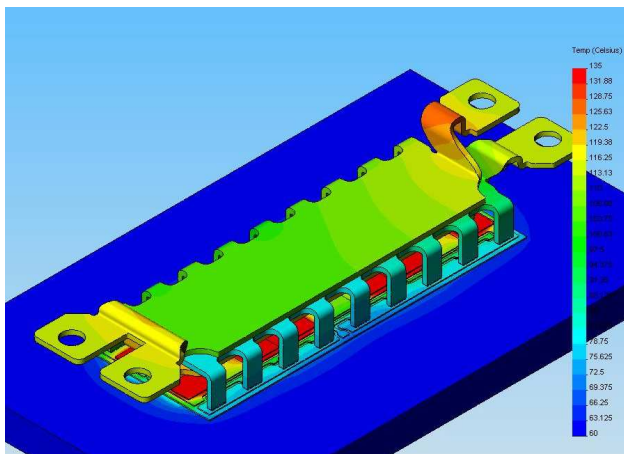


Fig. 6 Terminal temperatures at 600Arms AC-terminal current

This limit is above the expected continuous current under practical relevant operating conditions. But it could be reached with low switching frequencies and excellent cooling. The high current goes along with high power dissipation in the semiconductors, which has also a strong influence on the terminal temperature. This was taken in consideration for the Simulation in Fig. 6 with a power dissipation of 1900W per Inverter phase leg. The terminal temperature could be kept in that case below 125°C .

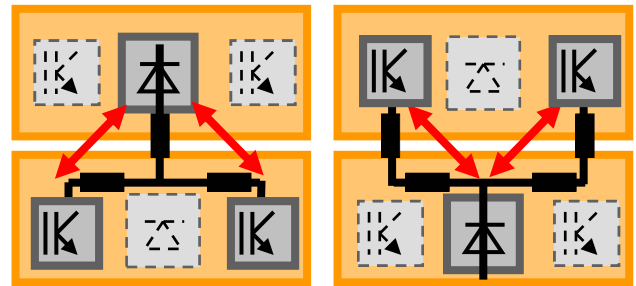
3 DBC Layout

The Layout of the DBC substrate and the chip position has an important influence on the switching behaviour and the thermal resistance of the power semiconductors. Furthermore is it possible to improve the effectiveness of the temperature protection with a proper sensor position.

3.1 Switching behaviour

The switching behaviour is depending from the semiconductor properties but also strongly from the module design. Voltage drops caused by parasitic inductances can be responsible for different switching speed and oscillations between parallel chips even if the semiconductors have identical properties. To assure synchronous and "clean"

switching the parasitic inductances should be as small as possible and with the same effect on all semiconductors. The DBC design with a basic "building block" of two IGBT at the right and left side and a free wheeling diode between can fulfill this requirement. The current commutation path from the diode to the IGBT and reverse is as short as possible (see Fig. 7) and similar for top and bottom switch.



BOT-IGBT to TOP Diode TOP-IGBT to BOT Diode

Fig. 7 Commutation path between IGBT and Free wheeling diode for Top- and Bottom-switch

Figure 8 and 9 are showing switching waveforms of the 1200V SKIM63 module at 600A and 900V DC. Switching losses, over voltages and di/dt are almost identical for the Top- and the Bottom-IGBT. The difference in the voltage peak between top and bottom turn-off is only 15V (1,3%)

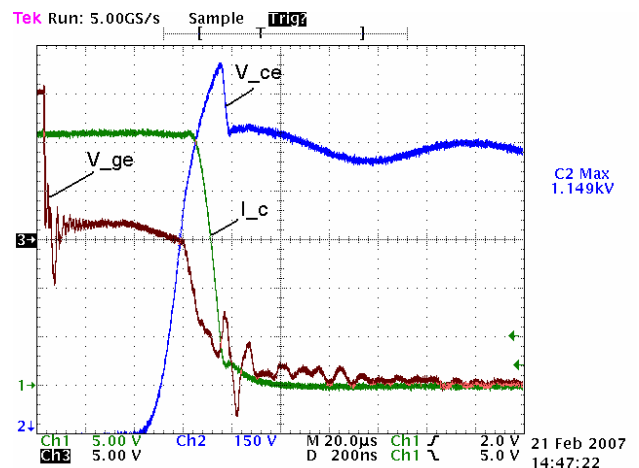


Fig. 8 Bottom IGBT turn-off switching waveform with double rated current 600A (green), V_{CE} (blue), V_{GE} (brown) @ $900V_{DC}$, 125°C

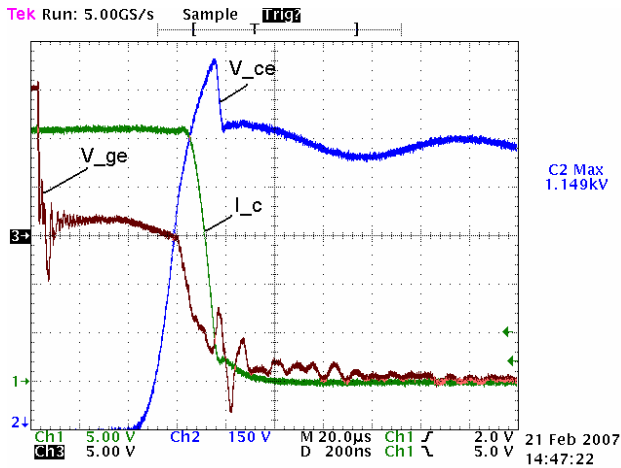


Fig. 9 Top IGBT Turn-off switching waveform with double rated current 600A (green), $-V_{CE}$ (blue), @ 900VDC, 125°C,

Furthermore a good dynamic current sharing between parallel IGBT has to be assured for similar switching losses in the chip. The distribution of the semiconductor parameter can cause mismatch of the switching losses in the range of 10%. An additional mismatch in the same or even higher range can be caused by an unsymmetrical device construction.

Two things have to be considered. At first different inductances in the chip current path from + to - DC, and second the voltage drop in the Gate control path, caused by the di/dt of the main current during switching.

The first problem is solved by the sandwich structure of the DC busbar. Figure 10 shows an equivalent circuit with lumped elements for the stray inductances. The IGBT on the DC terminal at the right hand side seems to have a lower inductance in the current path. But there is only a small change in the magnetic field along the sandwich, when the current commutates from + to - DC. The blue (grey) colored inductances are coupled and can be neglected. Removing it from the equivalent circuit (Fig. 11) it shows that the effective inductance is equal for all chips. It is independent, if the chip is located close to the DC terminal or at the AC terminal. This corresponds well with minimal measured voltage difference at turn-off (Fig. 5).

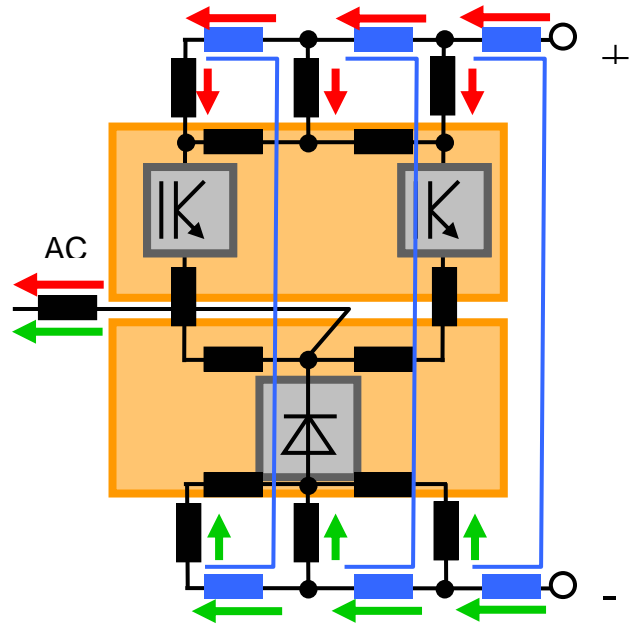


Fig. 10 Complete equivalent circuit with parasitic inductances for current commutation during switching

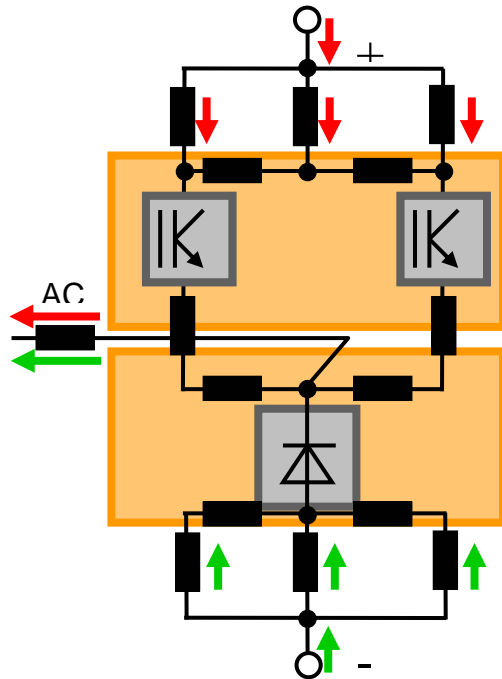


Fig. 11 Equivalent circuit with parasitic inductances for current commutation during switching without coupled inductances

The second effect was also taken into account by the chosen design, all IGBT see the same Gate Emitter voltage. In Fig 12 a situation is shown with the Gate Emitter voltage during turn-on of the TOP IGBT.

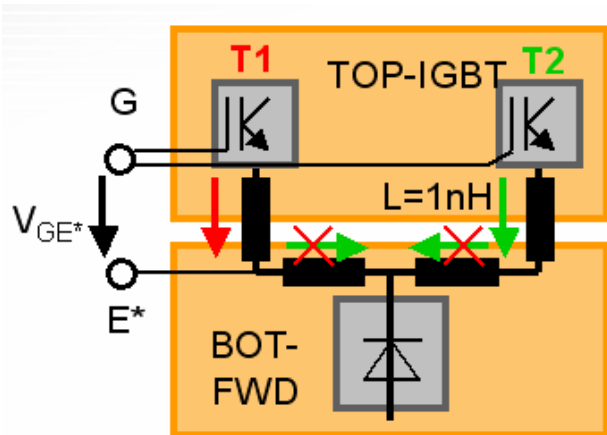


Fig. 12 Gate voltage conditions during switching

The voltages, induced by the parasitic inductance and the di/dt along the copper trace of the DCB, are in reverse direction for Transistor T2 and neutralize each other. Only the voltage along the bondwire inductance is subtracted from the applied gate voltage, but for all parallel IGBT in the same way. Equal current sharing during switching and even under short circuit conditions are the result.

3.2 Thermal resistance

Low forward voltage drops and junction temperatures of 175°C with the newest generations of power semiconductor allow very high nominal currents. The nominal current density can be higher than $2\text{A}/\text{mm}^2$. The chip size has to be chosen carefully for an optimised trade-off between nominal device current, cooling requirements and costs.

The thermal resistance is a function of the chip area but also from the distance between the chips (see Fig. 13). Large chips have a high temperature gradient across the chip itself and a bad heat spreading across the module mounting area. It can be shown that several chips with a smaller total area but some distance have a lower thermal resistance than 1 large chip. At distances below 3mm between two chips the thermal coupling is strong, above 3mm it disappears more and more.

But with small chips a lot of active chip area gets lost because of the additional chip edges. Higher losses at the same current are the consequence of a smaller chip area. A good compromise was found for these SKiM devices with chip sizes between 60 and 80mm^2 and a distance of 3mm between the chips for heat spreading.

The pressure contact beside of each chip prevents a bending of the cooling surface of the module. This allows minimizing the thickness of the thermal grease layer. Where for modules with base plate $80\dots 100\mu\text{m}$ are common, here only $20\dots 30\mu\text{m}$ are necessary.

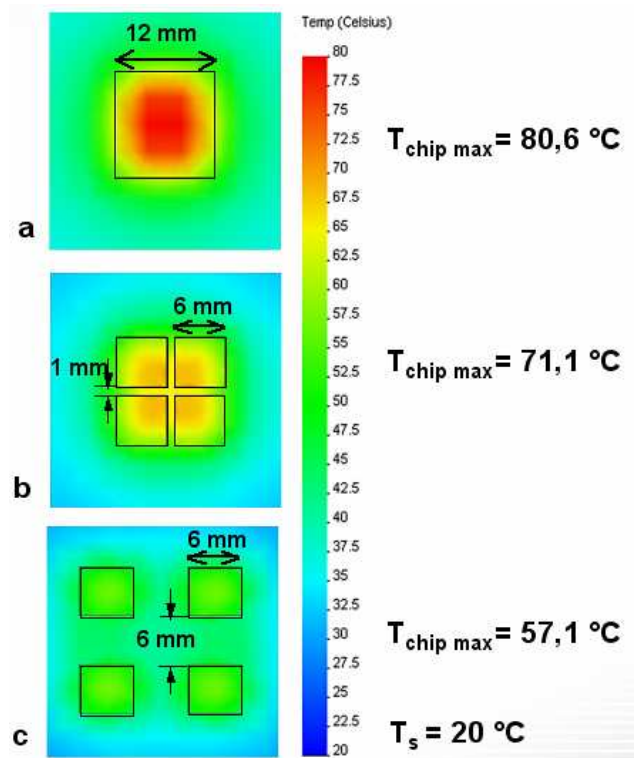


Fig. 13 Influence of heat spreading on the temperature of Chip with the same total area and power losses

The very thin sinter layer from silver with a high thermal conductivity reduces the thermal resistance slightly compared to a solder layer. An effect can also be seen from the massive copper terminals. They act like a heat spreader and conduct heat from the hotter center position to the cooler outer position. The result is a reduction of the effective thermal resistance between 5 and 10 %.

3.3. Device protection

A temperature sensor for device protection is integrated. The sensor position inside of a module has a higher influence on its suitability for temperature protection than the sensor tolerance. Especially if a hardware trip level is set by a driver or controller circuit. Different sensor positions were investigated in a case study. A model of a SKiM6 DCB is shown in Fig. 14. The thermal coupling of the sensor varies from A) direct at the same copper layer with the power semiconductors, over B) and C) insulated at different positions inside of the module to D) beside of the module at the heatsink.

Each sensor has a different thermal resistance junction (j) to sensor (r) $R_{th(j-r)}$ because of its different thermal coupling. A trip level for over temperature protection can be set under quasi static conditions for each of these sensors.

Unfortunately changes the $R_{th(j-r)}$ for other cooling condition (heatsink material and root thickness,

cooling medium, thickness of thermal grease...) and the trip level had to be set to new values. A better coupling between source and sensor reduces the influence of the cooling system and therefore the need to adapt the protection to the thermal stack.

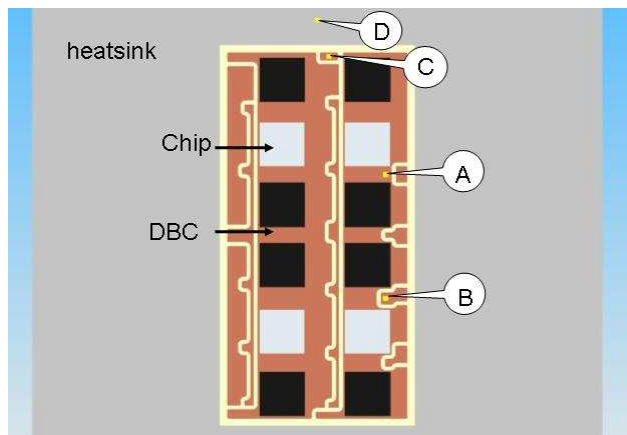


Fig. 14 Case study about different temperature sensor positions inside a power module;

To show the influence of the cooling system the thickness of the thermal grease layer was increased from nominal 25µm to 50µm. The change in the $R_{th(j-r)}$ is shown in Fig 15.

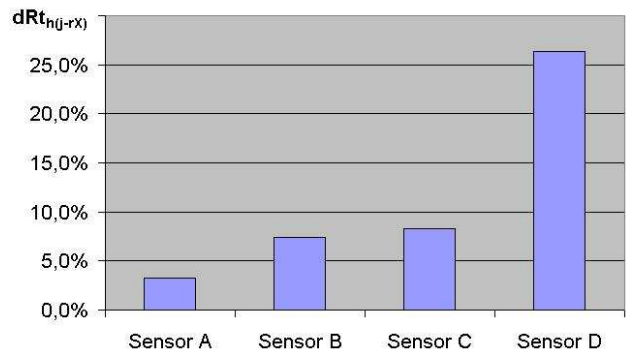


Fig. 15 Change of the thermal resistor junction to sensor caused by a doubled thickness of the thermal grease layer in percent.

A better thermal coupling between sensor and power semiconductor has also advantages in relation to dynamic protection at short overload conditions.

An overview about the advantages and disadvantages of the different sensor positions is given in table 2. For many reasons is the usage of a temperature sensor inside of the module recommended. Because of its insulation a sensor at position B) is the most preferred and was chosen for the SKiM modules. Future driver concepts with protection circuits and signal transforming at the driver secondary side could take advantage of sensor position A).

	Sensor A	Senor B	Senor C	Sensor D
thermal coupling to power semiconductors	Excellent	Acceptable to diodes and IGBT	Acceptable to IGBT, insufficient to diodes	Low
reaction time on overload pulses	Fast	Medium	Medium, higher than B	Low
influence of external cooling system	Low	Medium,	Medium, higher than B	High
Insulation	No, additional measures necessary	Basic, additional measures for safe insulation necessary	Basic, additional measures for safe insulation necessary	Safe insulation

Table 2: Comparison of different temperature sensor position with regard to suitability for power semiconductor protection

5 Packaging technology /Reliability

The extreme temperature cycling requirement excludes traditional Copper baseplate power module designs. Different thermal expansion coefficients stress interconnections between different materials. AlSiC is a reliable alternative but has a high cost impact. Furthermore it solves only the passive temperature cycling problem. A base plate less

pressure contact module is the presented alternative. A design with multiple electrical pressure points next to the paralleled chips, assure a low thermal resistance and homogeneous heat distribution. Both leads to lower temperature swings at the same changes in power dissipation, compared to traditional module designs. Lower temperature differences increase the lifetime of the device.

To improve the power cycling reliability even at high junction temperatures low temperature sintering

technology is used to attach the chips to the DBC substrate. A solder joint degrades during load cycles, which will lead to increased thermal resistance and module failure. The sinter joint is a thin silver layer that has a superior thermal resistance than solder and at the same time due to the high melting point of silver (960°C) no joining fatigue can be observed (see figure 16) leading also to an increased lifetime of the over all system [2].

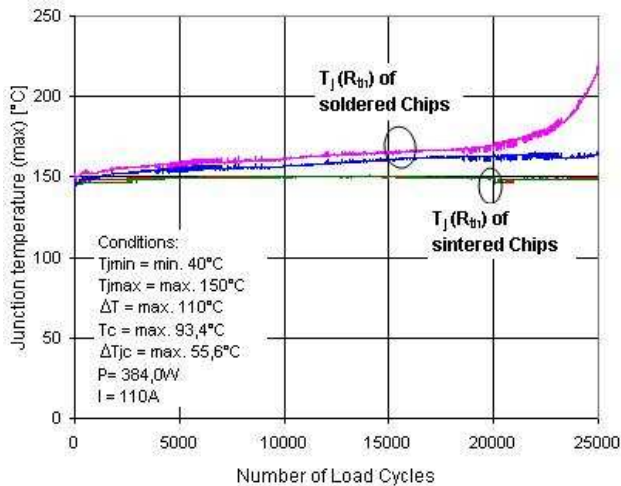


Fig. 16 Comparison of soldered and sintered chips in a temperature cycling tests

Due to the pressure and spring contact and the sinter technology used for chip attach these modules are completely solder free power modules.

6. Conclusion

A new power module optimized for the requirements of automotive applications was introduced. It is the first 100% solder free isolated IGBT module using pressure contact and sinter technology. This assures a high active and passive temperature cycling capability. The device design was optimized with respect to low thermal resistance and symmetric current sharing between parallel chips. This allows together with the maximum junction temperature of 175°C a compact inverter design with a high power density.

7. References

- [1] W. Tursky, P. Beckedahl, SEMIKRON International: "Advanced Drive Systems", IEEE PESC/CIPS 2004, Aachen, conference proceedings
- [2] C. Göbl, "Low temperature sinter technology die attachment for automotive power electronic applications" APE 2006, Paris, conference proceedings

8. Glossary

- SKiM - Semikron Integrated Module
- DBC - direct bonded copper (ceramic substrate)
- CTE - Coefficient of Thermal Expansion
- NTC - Temperature Sensor with "Negative Temperature Coefficient"
- PCB – Printed Circuit Board
- FEM – Finite element method (Simulation)
- AIPM – Automotive Intelligent Power Module
- EMI – Electro Magnetic Interferences
- AlSiC – Aluminum Silicon Carbide Alloy