One screw mounting SEMITOP power module design

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**SEMIKRON expands the SEMITOP® family and thereby increases the power range with the introduction of the SEMITOP® 4 with a power capability of up to 22 kW motor power.
It is fully compatible to the existing SEMITOP® 1, 2 and 3 modules. The module is available in 3-Ø IGBT and MOSFET inverter and in Converter Inverter Brake topologies. The maximum power rating of an IGBT inverter in SEMITOP® 4 is over three times compared to standard inverters in SEMITOP® 3. A different substrate with improved thermal performances has been used in order to achieve this result. SEMITOP® 4 has been designed using a mechanical and thermal finite element simulation software to meet any critical mechanical and thermal aspects, even under the worst environmental conditions. With the help of this software a different approach to power electronics design has been implemented.**

Power electronic applications are continuously demanding cost-effective power modules with increased efficiency and performances. Because of increased power density and cost containment of power electronic applications, thermal calculation and electrical dimensioning of new power modules, design is becoming even more important than in the past since temperature safety margins in the power modules' design are continuously decreased [1], [2], [13], [14].

This trend of continuous reduction of the safety margins, makes the knowledge of "secondary" thermal issues (thermal crosstalk, temperature contours distortion and border effects) and their combinations important to achieve a successful design and a reliable power module. Taking these facts into account SEMIKRON designed the new SEMITOP® 4 (Fig. 1). This module has been designed using a mechanical and thermal finite element simulation software. This new module without baseplate and one screw mounting enhance the SEMITOP® family increasing the power range with a cost-effective solution.

SEMITOP® 4, the technology

The new module with outline dimensions: W=60mm L=55mm H=12mm (Fig. 1) is fully compatible with SEMITOP® 1, 2 and 3 i.e. is it possible to use in combination with the existing SEMITOP® 1, 2 and 3 on the same circuit board and on the same heat-sink [3].

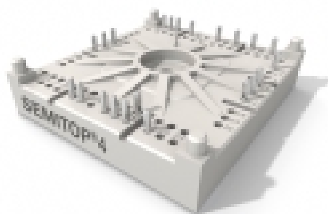

Fig. 1. SEMITOP® 4

The module is available in 3-Ø IGBT (and MOSFET) inverter and in Converter Inverter Brake topologies. The present SEMITOP® 4 product portfolio is listed in Table 1. As specified in Table 1 is the maximum power rating for IGBT inverter and CIB topologies in SEMITOP® 4 housing between 3-4 times higher than the IGBT inverter in SEMITOP® 3. The power density in the IGBT inverter in SEMITOP® 4 is increased up to 47% compared to SEMITOP® 3 for 600V and is increased up to 38% compared to SEMITOP® 3 for 1200V.

	I_C @ T_S=25°C	I_C @ T_S=80°C
GD126 Version		
3-Ø 1200V IGBT Inverter	100A	70A
3-Ø 1200V IGBT Inverter	77A	53A
3-Ø 1200V IGBT Inverter	65A	43A
GD066 Version*		
3-Ø 600V IGBT Inverter	155A	110A
3-Ø 600V IGBT Inverter	117A	82A
3-Ø 600V IGBT Inverter	84A	55A
DGDL126 Version		
CIB 1200V	60A	40A
CIB 1200V	45A	30A
DGDL066 Version*		
CIB 600V	90A	70A
CIB 600V	75A	56A
MD Version		
3-Ø 100V MOSFET Inverter	165A	125A
3-Ø 55V MOSFET Inverter	225A	170A

* $T_{J(MAX)}$ = 175°C

Table 1. SEMITOP® 4 product portfolio.

To achieve these features, a substrate with different thicknesses of insulator and copper topside/backside and improved thermal performances has been implemented. The substrate chosen has a thickness of 0,38mm aluminium oxide (Al_2O_3) with Curamik® pre-bent technology [4]. This substrate is especially suitable for modules without baseplate and allows an even thermal paste distribution as well as 100% adhesion of the power hybrid's backside to the heat-sink surface although the module has only one screw mounting. The thermal paste thickness does not need to be increased compared to SEMITOP® 3.

With this new substrate the thermal resistance of IGBT is reduced by up to 20%. For instance, SK75GD126T inverter in SEMITOP® 4 (1200V / 75A at T_S=80°C) has a typical thermal resistance of 0,39K/W. The same silicon dice mounted into SEMITOP® 3 shows a typical $R_{th(j-s)}$=0,49K/W, with a reduction of about 20%. Special emphasis has been dedicated to the mechanical and thermal design of this module.

Mechanical simulations and design

To meet increased quality requirements and avoiding critical aspects in terms of substrate mechanical stress, a finite element mechanical analysis on different shapes, structure and housing materials has been performed [5]. This analysis reduced expensive tests usually performed during building trial housings made by milling machines and testing plastic mould tooling. Moreover these simulations reduced the time for prototyping and time-to-market for the final product.

In Fig. 2 the exaggerated mechanical deformation of a SEMITOP® 4 housing prototype made in standard polymer (ABS) is shown. It is easy to see that this leads to excessive deformation of the housing (over 1,3mm) applying the nominal torque to the centre screw. Using GF reinforced materials and other special plastic materials an even mechanical pressure distribution with great containment of housing deformation has been achieved.

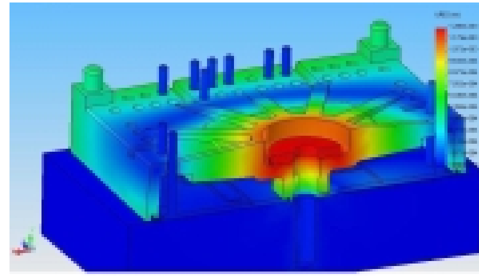

Fig. 2. Mechanical deformation and pressure distribution on SEMITOP® 4

Thermal simulations and design

As mentioned above, due to increased power density and cost containment of power electronic applications, thermal calculation and dimensioning of new power modules design are becoming more and more important. It is therefore absolutely necessary that extensive information is needed of the "secondary thermal phenomenon" such as thermal transients, thermal crosstalk, temperature contours distortion and border effects for each layout designed, mainly for dice paralleling [6], [7], [8], [9], [13], [14] Up to now, the calculation on thermal resistance for dice paralleling has been done simply by using de-rating factors based on measurements. Whilst the influence of "border effect", "thermal crosstalk", "deformation of temperature contours" and the modulation of all these effects were substantially neglected [7].

With the introduction of the user-friendly finite element software [11] and the increasing power calculation of PCs it has been possible to generate finite element models (FEMs) in a short time starting from 3D-files or 2D-CAD files and so getting a complete and detailed substrate layout analysis in a few hours. This allowed a time-effective generation of a great number of FEMs and then huge numbers of data to manage (which was impossible up to now with standard FE software and PCs since for a complete FEM took days).

SK100GD126T IGBT=2×57mm^2 FWD=61mm^2	Measured $R_{th(j-s)}$ [K/W]	FEA $R_{th(j-s)}$ [K/W]	Diff [%]
IGBT (top 1)	0,42	0,427	1,6
IGBT (top 2)	0,39	0,397	1,8
IGBT (top 3)	0,41	0,403	-1,7
IGBT (bottom 1)	0,44	0,437	-0,7
IGBT (bottom 2)	0,39	0,393	0,8
IGBT (bottom 3)	0,43	0,436	1,4
FWD (top 1)	0,62	0,625	0,8
FWD (top 2)	0,61	0,621	1,8
FWD (top 3)	0,69	0,686	-0,6
FWD (bottom 1)	0,67	0,674	0,6
FWD (bottom 2)	0,68	0,669	-1,6
FWD (bottom 3)	0,68	0,675	-0,7

Table 2. Comparison between measured $R_{th(j-s)}$ and simulated $R_{th(j-s)}$ for each IGBT and FWD (SK100GD126T).

It has been possible to verify the $R_{th(j-s)}$ distribution for each customized layout and the identification of every possible thermal critical aspect. The eventual critical points are then usually discussed with the final customer to evaluate the effective critical response on the real application. In Table 2 are the measured values of $R_{th(j-s)}$ [12] for each IGBT and each FWD compared to the related FEA results, and it is easy to verify the consistency of the simulation results.

In the second case it is important that the chosen measurement points (for the T_J and for the T_s) have the same plane (X- and Y-) coordinate, varying only the vertical Z-coordinate (see Figs. 3.a and 3.b). The temperature on a silicon die (and mainly in paralleled dice) can even vary several degrees (for instance in Fig. 3.a T_J varies from 114°C to 96°C) and then the manual incorrect choice of measurement points can falsify the simulation result [10].

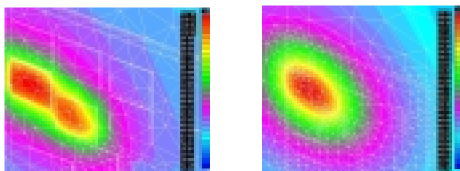

Fig. 3. $R_{th(j-s)}$ measurement at P_D=121.6W.
3.a Junction temperature contour ($T_{J(max)}$=111.47°C)
3.b heat sink temperature contour ($T_{s(max)}$=59.47°C) on switch $IGBT_{TOP1}$ SK100GD126T.

A completely different scenario is reported in the Fig. 4 where a simulation of the same module running in a standard motor control application is shown. In this figure the great differences of the dynamic $R_{th(j-s)}$ values during working operating condition due to thermal interference, temperature contours distortion and lower P_D per IGBT and FWD are quite evident. As additional information, Fig. 4 also shows the temperature sensor which is positioned at the upper right corner of the power hybrid. With the FEA it is possible to check the real temperature "seen" by the temperature sensor (96°C, which is about 17°C less than the hottest point in the module) and to compare it with the switches temperature to give a more accurate figure of the T_J situation instead of having the usual general indication of the power hybrid's temperature.

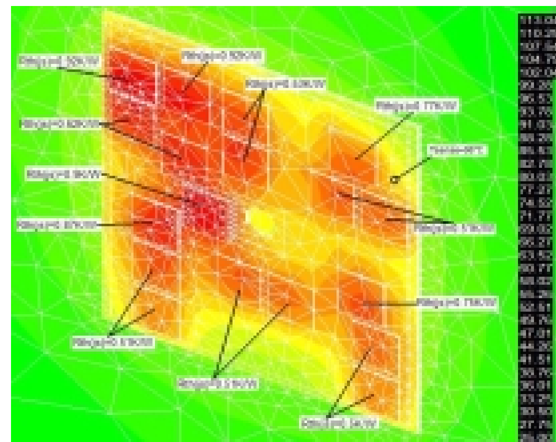

Fig. 4. Simulation of SK100GD126T module running in application with specification of each $R_{th(j-s)}$.

New coefficients for fast $R_{th(j-s)}$ calculation

With the help of the software it has been possible to introduce new de-rating coefficients for the calculation of fast power hybrids $R_{th(j-s)}$ which take into account the "secondary thermal phenomenon" impact and their combination.

For example, Fig. 5 shows the $R_{th(j-s)}$ as a function of dice distance for two paralleled dice (keeping a minimum distance die to border >5mm) and for four paralleled dice (Fig. 6) mounted on standard alumina substrate [4]. The consistency of these graphs have been proved by comparing measurements to SEMITOP®3 and SEMITOP®2 modules following international standard for R_{th} and Z_{th} measurement: IEC 747-8/2.18.

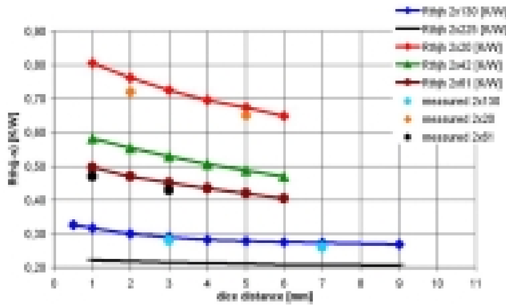

Fig. 5. $R_{th(j-s)}$ as a function of dice distance for two paralleled dice and different die size.

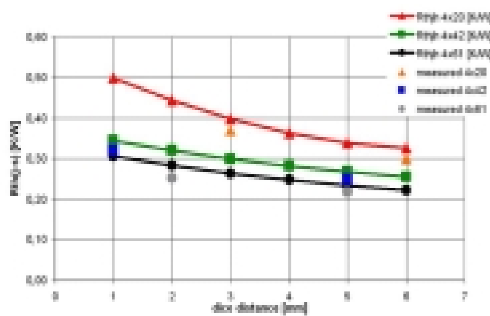

Fig. 6. $R_{th(j-s)}$ as a function of dice distance for four paralleled dice and different die size.

Furthermore, during simulations it has been found that de-rating factors are strongly influenced by the dice shape and distance of the dice to the substrate border. Indeed, it can happens that, at the same power dissipation level and measurement conditions, paralleled dice with adjacent shorter side in rectangular shape show an $R_{th(j-s)}$ reduction between 5% to 16% than paralleled dice with adjacent longer side. This percentage of course increases in function of the number of paralleled dice and decreases in function of dice distance. Fig. 7 shows the $R_{th(j-s)}$ as a function of dice distance and as a function of adjacent side length. In particular, the position of paralleled dice is specified in the graph's legenda. This is mainly due to the combination of deformation of temperature contours and interference phenomenon (the simulation was done trying to avoid border effect using distance dice to border >5mm).

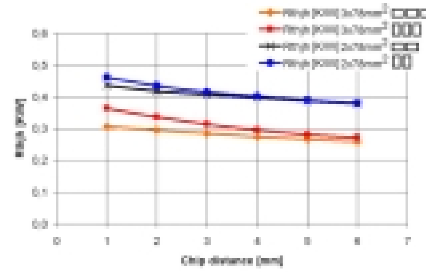

Fig. 7. $R_{th(j-s)}$ as a function of dice distance and as a function of adjacent dice side length.

Then, it's easy to understand that R_{th} in paralleled rectangular dice is smaller than the R_{th} in paralleled square dice at the same measurement conditions and at the same total switch silicon effective area.

Test results and reliability

The reliability tests have been performed according to international standards listed in Table 3 [3].
These tests validate and confirm SEMITOP® performances and reliability. Special emphasis was placed on thermal cycling, power cycling and mechanical tests.

Test	Conditions
High Temperature Reverse Bias (HTRB) *IEC 60747*	1000 h, 95% V_{DSmax}/V_{CEmax}, 125°C ≤ T_c ≤ 145°C
High Temperature Gate Bias (HTGB) *IEC 60747*	1000 h, ± V_{GSmax}/V_{GEmax}, T_{vjmax}
High Humidity High Temperature Reverse Bias (THB) *IEC 60068-2-67*	1000 h, 85°C, 85% RH, V_{DS}/V_{CE} = 80% V_{DSmax}/V_{CEmax}, max. 80V, V_{GE} = 0V
High Temperature Storage (HTS) *IEC 60068-2-2*	1000 h, T_{stgmax}
Low Temperature Storage (LTS) *IEC 60068-2-1*	1000 h, T_{stgmin}
Thermal Cycling (TC) *IEC 60068-2-14 Test Na*	100 cycles, T_{stgmax} - T_{stgmin}
Power Cycling (PC) *IEC 60749-34*	20.000 load cycles, ΔT_j = 100K
Vibration *IEC 60068-2-6 Test Fc*	Sinusoidal sweep, 5g, 2 h per axis (x, y, z)
Mechanical Shock *IEC 60068-2-27 Test Ea*	Half sine puls, 30g, 3 times each direction (±x, ±y, ±z)

Table 3. Reliability tests.

Conclusion

SEMIKRON expands the SEMITOP® family (without baseplate, one screw mounting modules) with the introduction of the new SEMITOP® 4. A different substrate with improved thermal performances has been used. The maximum power rating of IGBT inverter in SEMITOP® 4 is over three times compared to present SEMITOP® 3 inverters. These modules have been designed using mechanical and thermal finite element simulation software to meet any critical mechanical and thermal aspect, even in the worst environments. With the help of this software a different approach to power electronics design has been implemented.

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