Power Module Design without Solder Interfaces – an Ideal Solution for Hybrid Vehicle Traction Applications

U. Scheuermann
SEMIKRON Elektronik GmbH & Co. KG
Sigmundstr. 200
90431 Nuremberg, Germany

Abstract — **Hybrid vehicle traction applications require compact power modules with high reliability. A major challenge is the lifetime under thermal cycles. While the requirements are moderate with respect to (active) power cycles, there are challenging requests for a high lifetime under (passive) temperature cycles. Base plates and solder interfaces limit the stability for temperature cycles in the classical module design. Advanced module architecture without base plate and without a single solder interface overcomes the limits of the classical module design and provides an ideal solution for hybrid automotive traction systems.**

I. INTRODUCTION

Power semiconductor modules must be capable to withstand the stress induced by thermal cycles in every application. These thermal cycles are caused by active power cycles on one hand, when thermal losses are generated inside the power chips by conducting high currents or by switching the current on and off. On the other hand, passive thermal cycles are occurring due to changes in the environmental temperature, which could be either changes in the ambient temperature or temperature excursions of the system environment like the change of heat sink temperature or of the cooling liquid.

While both active and passive thermal cycles are limiting the lifetime of power modules in every application, hybrid automotive traction systems represent a unique challenge for the module reliability because the requirement to endure passive thermal cycles is much higher than in conventional industrial applications.

If we expect a modern car to run for 300,000 km in its lifetime and we assume an average velocity of 30 km/h, then the lifetime would add up to only 10,000 hours in operation. Nevertheless, this operational lifetime consists of a couple of thousand individual start-stop cycles. Hence, the capability to withstand passive cycles is the challenge for automotive hybrid systems.

From the technological point of view, any lifetime requirement can be achieved for active power cycles by simply increasing the silicon chip area. For passive temperature cycles in contrast, only the materials implemented with their specific coefficients of thermal expansion (CTE) and the interconnection technologies determine the lifetime of power modules under repeated temperature swings. Therefore, the passive temperature cycle lifetime requirement can only be met by a suitable module architecture.

II. LIMITS OF CLASSICAL MODULE DESIGN

In classical module design, the ceramic DBC substrates are connected to a solid copper base plate by a solder interface. This construction principle evokes numerous problems with respect to the thermal interface between the module case and the heat sink.

The difference in CTE between the substrate layer and the base plate material generates a camber of the base plate through the bi-metal effect, resulting in peaks of visco-plastic strain close to the edges of the substrates [1]. The shape of the base plate after the solder process in strongly influenced by the ceramic and base plate materials used and as well by the solder material applied [2]. This makes it very difficult to find an ideal shape for the base plate, which forms a perfect interface for the heat transfer to the heat sink in the complete operation temperature range [3]. It also limits the maximum size of substrates used in a base plate design. Moreover, the considerable stress established in the system after the solder process provokes a creep in the solder layer, which leads to a relaxation of the camber over time [4]. These effects together prevent the construction of a perfect thermal interface with a solid base plate.

However, the most severe consequence of the stress induced by CTE mismatch is the limitation of the lifetime during temperature cycles. Pronounced temperature gradients are imprinted in a classical module during active power cycles, so that the differences in CTE do not develop their total stress potential [5]. During passive temperature cycles in contrast, the maximum and minimum temperatures are reached by all composition layers, evoking the full stress potential in the system. This makes passive temperature cycles the critical test for the module architecture.

Fig. 1 shows a Scanning Acoustic Microscopy (SAM) images of a classical 32 mm base plate module with 0.3/0.38/0.3 mm Al_2O_3 substrates and a conventional 3 mm copper base plate after 200 cycles in a two chamber temperature shock test with chamber temperatures of -40 °C and +125 °C and dwell times of 90 minutes in the hot and 90

minutes in the cold chamber. Fig. 1a shows the SAM image of the base plate to substrate solder interface. The reflections of the acoustic waves, indicated by the light areas, show the delaminations in the solder interface beginning at the corners of the substrate and moving inwards.

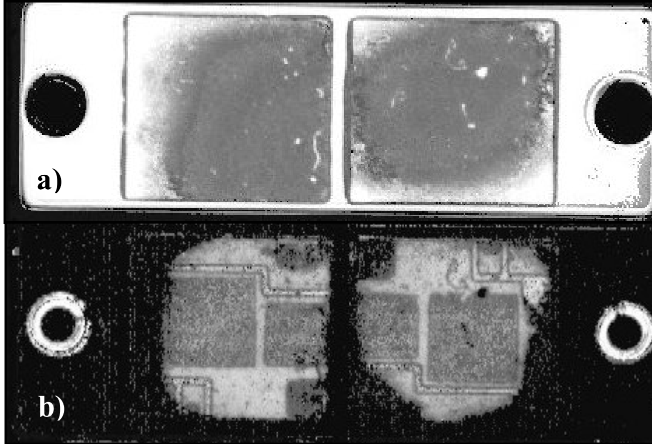

Fig. 1: Scanning Acoustic Microscopy (SAM) images of a classical 32 mm power module with base plate after 200 temperature cycles in a two-chamber temperature shock test (-40 / +125 °C). a) Solder interface base plate to substrate b) solder interface substrate to chip.

Fig. 1b shows the SAM image of the solder interface between the substrate and the chip. The acoustic waves enter the module from the base plate side and the reflected signal is recorded from this side as well. Therefore, delaminations reduce the signal strength and prevent to gain information from deeper layers. The black areas in Fig. 1b at the substrate position thus indicate areas of high delamination in the substrate to base plate interface. This artifact is convenient, because it allows evaluating how close the delamination is already progressed with respect to the chip positions. The SAM image verifies that the delimitation has almost reached the chip positions. Further passive temperature cycles will drive these delaminations between substrate and base plate underneath the chip positions. This would interfere with the thermal path and increase the thermal resistance of the chips, resulting in higher junction temperatures and accelerate the degradation of the power module in a real application.

One strategy to overcome this limitation is to minimize the stress between the substrate and the base plate by replacing the conventional copper base plate material with a material featuring an adapted CTE [6]. Although this system design is well established for AlN-substrate modules by implementing AlSiC base plates, the reduced thermal conductivity of such a tailored material is increasing the thermal resistance of the package and therefore impairs the thermal performance.

III. The Pressure Contact Technology

A different approach is the pressure contact technology, which eliminates the base plate. The technology is also established for years in many power electronic applications; it was first introduced in the SEMIKRON SKiiP system. Any desired ceramic substrate can be implemented in this system, because the lack of rigid interconnection eliminates the need for a CTE adaptation. So Al_2O_3 or AlN substrates can be used for the package without any adaptation of the module architecture [7]. Additionally, the substrate size is no more restricted to maximum limits and large area substrates can be implemented and make numerous interconnections between individual small substrates obsolete.

Fig. 2 shows a cross sectional view of the SKiiP pressure contact system. A non-conductive bridge element transfers the force from the pressure system, consisting of a rigid pressure plate and a pressure foam layer, to the substrate. The pressure system also presses the load contacts to the substrate. It thus establishes the thermal contact and electrical contacts at the same time.

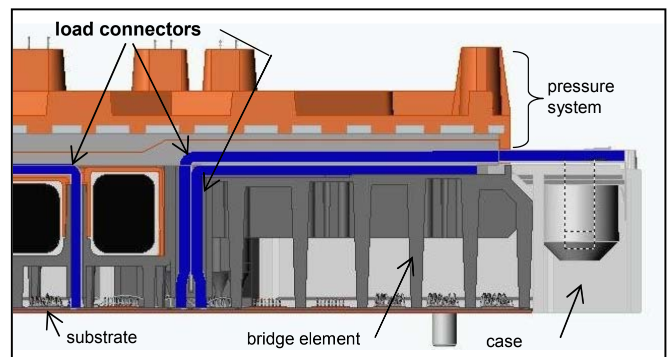

Fig. 2: Design of the pressure contact system of the SKiiP System. The cross section shows the bridge element, the pressure system and the load contact together with the power substrate.

The application of these pressure contact designs with the flexibility to implement different ceramic substrates in the field has proven the reliability and potential of this design [8].

When these first pressure system designs were developed, an important synergy effect was not anticipated: It is advantageous to replace the bridge element by a multi contact bus bar structure for the load contacts as shown in Fig. 3. In this design, mechanical pressure to assure a good thermal contact of the substrate to the heat sink is transferred by

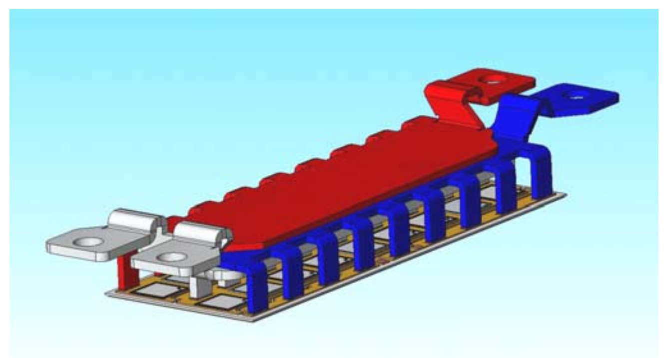

Fig. 3: Improved pressure contact system with multiple load contacts in a bus bar structure. The drawing shows the plus contacts (red), the minus conatc (blue) and the AC-contact (grey) of a SKiM93 phase leg, establishing both mechanical (thermal) contact and current contacts.

multiple load current connectors of the internal bus bar system. This concept exhibits fundamental advantages for the static and dynamic current sharing for paralleled chips.

First, a simulation of current sharing in a SKiM®63 module will illustrate the advantage for the static current sharing. Fig. 4 shows the current flow for the considered example. The current is fed in through the +DC connector of the first phase leg. The current branches through the parallel connected TOP IGBTs and is collected by the AC trace. From here it flows to the external AC terminal which is connected by a bridge with the AC terminal of a second phase leg. From there the current branches through the BOT IGBTs of the second phase leg and is collected by the minus trace and conducted to the –DC terminal.

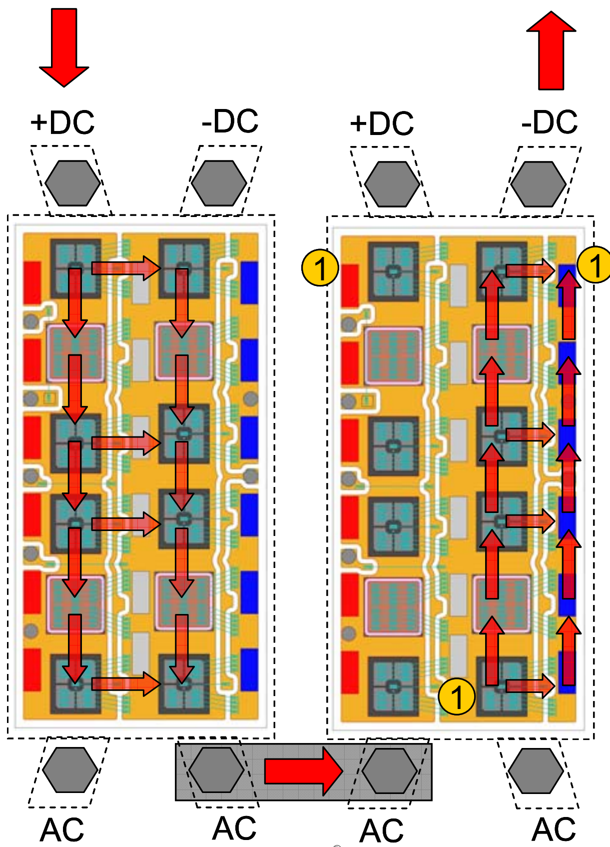

Fig. 4: Two phase legs of the SKiM®63 module with the current flow used for the simulation of the static current distribution.

In order to simulate the current distribution between the parallel chips, the path resistance on the DBC substrate as well as the path resistance of the bus bar structure was calculated from the geometry and the specific resistance of copper. The chips were assumed identical and their forward characteristic was approximated by a linear relationship between current and voltage drop, which describes the current voltage characteristic close to the nominal current sufficiently well. The resistance of the wire bonds was also calculated form their geometry and material parameters. Then, the so derived electrical equivalent network was calculated with PSPICE.

Fig. 5 displays the results for the SKiM®63 module with 4 chips per switch in parallel. The current deviates from the nominal 100 A per switch less than 0.3 A and thus shows an imbalance of approximately 0.3%.

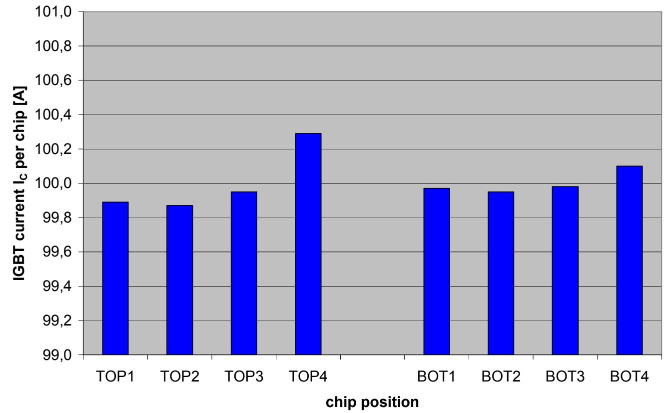

Fig. 5: Result for the static current sharing of a SKiM®63 module with pressure contact system with multiple contact points. The current imbalance is less than 0.3%.

To evaluate this result, a modified system was analyzed with the same simulation strategy. In contrast to the realistic bus bar contact system with multiple contacts, only a single contact spot on the DBC substrate was assumed (i.e. the first contact relative to the terminal of the original bus bar system). The positions are indicated by the circled 1 in Fig. 4. For the +DC and –DC connectors the position of the single contact was on the top side of the substrate, for the AC connector the contact was located at the bottom side of the substrate. Thus, each contact position was close to the related load terminal, which is a realistic assumption for conventional packages. The current distribution for this hypothetical system is depicted in Fig. 6.

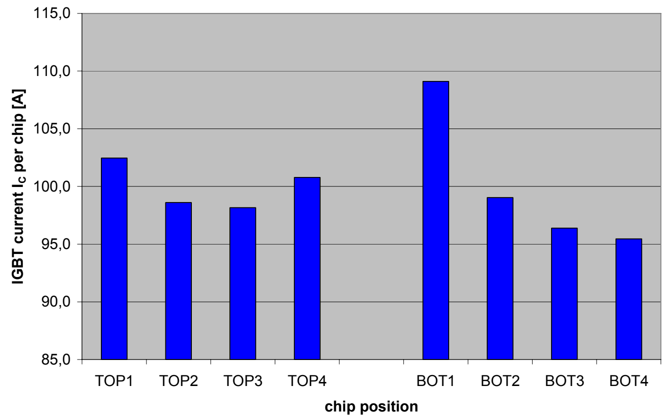

Fig. 6: Current distribution of a modified system. The same substrate and chips are used as in Fig. 5, but the current is supplied only by a single contact location, that is the first contact close to the related load terminal.

The current imbalance in this case amounts to 9%. The imbalance is especially pronounced for the BOT switch, reflecting the fact, that the minus trace on the DBC substrate is typically much smaller than the plus or AC trace, because no

chips are placed on this trace. The comparison shows, that the bus bar concept with multiple load contacts substantially improves the static current sharing in power modules with several parallel chips. An evenly balanced current sharing distributes the stress in application evenly between the chips and thus increases the reliability of the package, which is always determined by the weakest link of the chain.

Additionally to the static current sharing, the dynamic current distribution during switching is of great interest for a power module package. Fig. 7 shows the result of a dynamic measurement on a SKiM®63 phase leg. The voltage drop was measured at different chip locations during an IGBT turn-off with an dI/dt of 6600 A/µs for a DC link voltage of 700 V. The electrical potential was measured for the chip close to the AC terminal, for a middle position and for the chip located close to the DC terminals. The maximum voltages for all three positions, which appear as almost one single trace in the oscilloscope image, range between 929 V and 936 V, which is equivalent to a variation of parasitic inductance of less than 1 nH.

The dynamic measurement corroborates the statement of very homogeneous current distribution derived from simulation and illustrates the considerable improvement that the pressure system design in combination with an internal bus bar structure with multiple contacts exhibits in comparison to traditional power module designs.

IV. The Sinter Technology

With the replacement of the soldered base plate by a pressure contact technology, the limited reliability during passive thermal cycles is improved. Even if theoretically, any lifetime requirement during active thermal cycles can be achieved by implementing sufficient chip area, this is no possible solution for hybrid cars. The constrictions in space and weight available for the power electronic components require the highest possible package density. Additionally, the intention to use the combustion engine cooling system for the cooling of the power electronic components increases the requirements for the reliability during active power cycles. Maximum cooling liquid temperatures of 110 °C demand to utilize the power chips to the maximum of the operation temperature range, limited only by the maximum junction temperature of 175 °C. Under these boundary conditions, the reliability during active power cycles must be as high as possible for hybrid traction applications.

Therefore, the last remaining solder interface between the chip and the substrate was replaced by a superior interconnection technology: the silver diffusion sinter technique. This technology was originally developed to join large area round SCRs with molybdenum discs. In the middle of the 90s, first attempts were made to adapt the process to the interconnection of modern small size IGBT and diode chips to ceramic substrates [9].

Today, SEMIKRON has developed a process for the silver sinter technology compatible with the requirements of power module series production. The process allows joining a variety of different chips on a substrate in a single process step as shown in Fig. 8. On a 5” by 7” master card, 48 IGBTs, 48 small gate resistor chips and 24 freewheeling diodes (FWD) are connected via silver diffusion technique in this example. Thus, four phase leg substrates are assembled in a single process step.

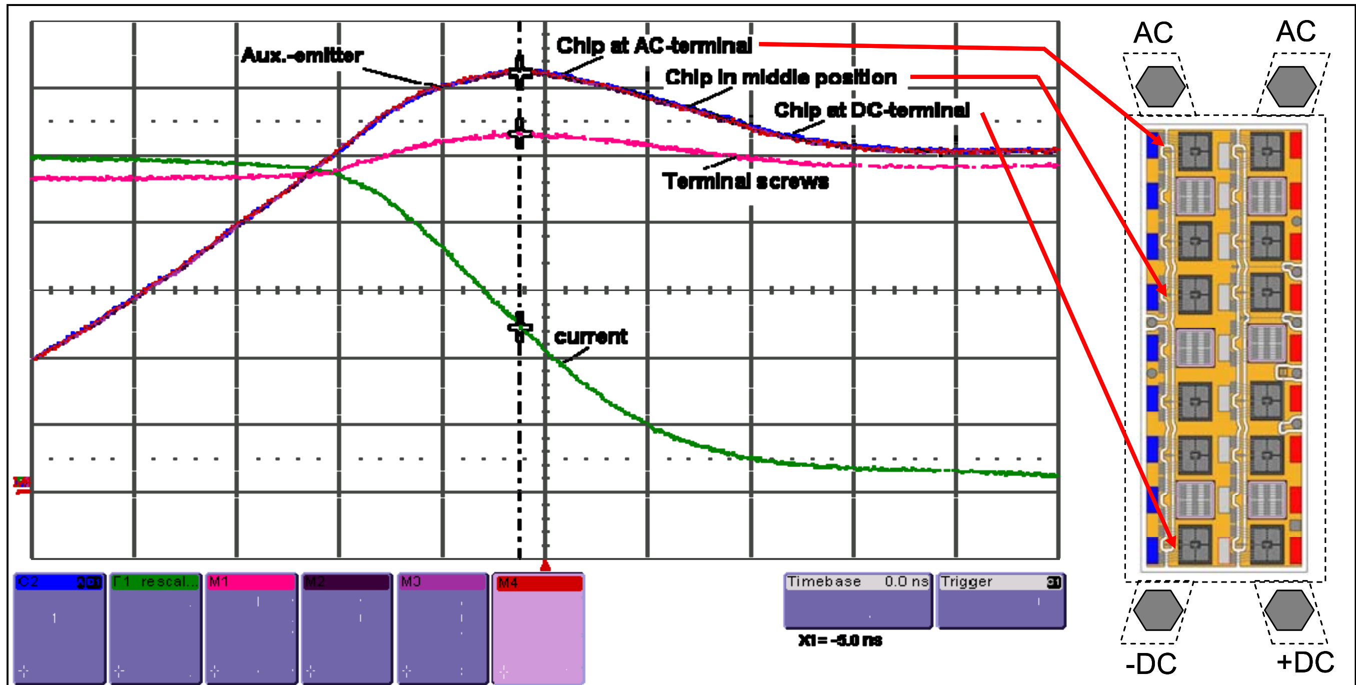

Fig. 7: Measurement of the potential at different chip positions during IGBT turn-off. The difference in over-voltage between the chip close to the AC terminal, a chip in a middle position and the chip at the DC terminals result in a parasitic inductance spread of below 1 nH.

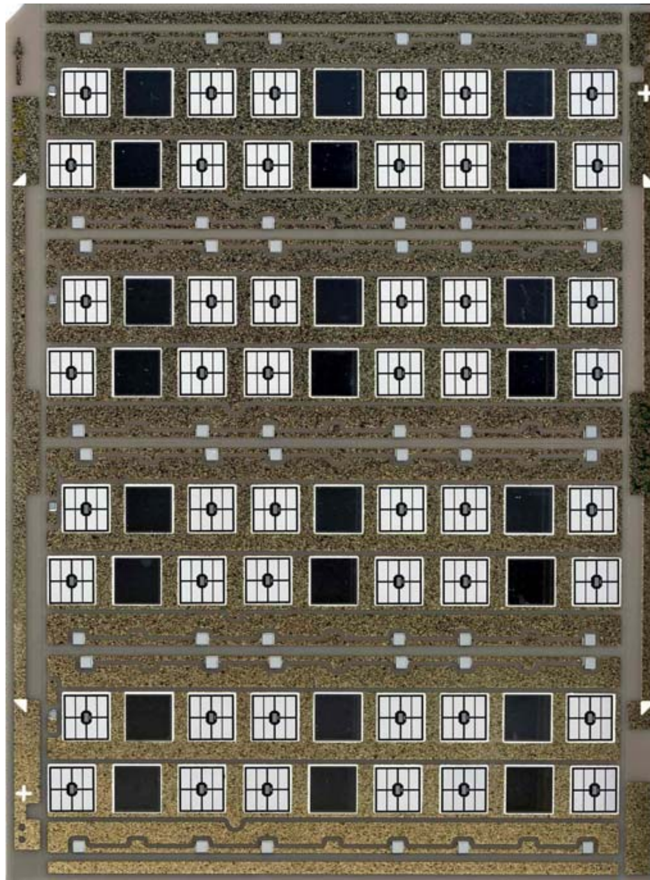

Fig. 8: 5” x 7” master card after the diffusion sinter process. 120 chips are connected to the substrate in a single process step.

For the sinter process, a paste is applied to the substrate. This paste consists of silver flakes embedded in a semifluid matrix. The silver flakes are coated with an organic protective cover to prevent an agglomeration before the process start. The chips are then placed into the paste, comparable to a solder paste process.

Then the assembled substrate master card is pressurized with a hydrostatic pressure in the range of 40 MPa while at the same time, the temperature is increased to 200-250 °C. The protective coating of the silver flakes is dissolved by the elevated temperature and assisted by the pressure, the particles are densified and diffuse together to form a porous interconnection layer as shown in Fig. 9.

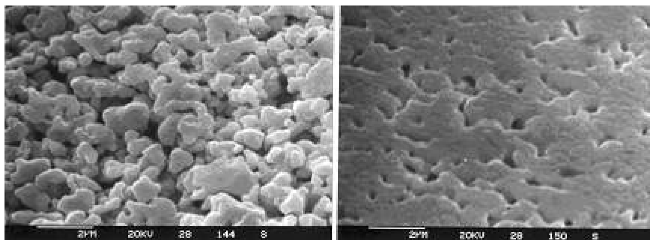

Fig. 9: REM image of the silver diffusion layer before (left) and after (right) the sinter process. Using a polished Si-surface instead of a noble metal contact prevents the formation of a connection.

Noble metal surfaces on both partners are required for the formation of an interconnection. In Fig. 9, a chip with a polished Si surface was used, so that no bonding between the silver sinter layer and the chip occurred. This allows to remove the chip after the sinter process and to evaluate the interface layer. The REM image shows, that a certain porosity remains in the silver diffusion layer.

The silver diffusion sinter technology has numerous advantages compared to the classical solder interface. First of all, no transition to a fluid phase occurs in the interface layer. During such a liquid phase as encountered in every solder connection, the chip floats on a liquid layer and can move or turn out of the desired position. The absence of a fluid phase transition in the sinter process prevents such a shifting of chips and allows to exactly position the chips at the desired location. Additionally, no voids can form in a silver sinter layer, only a homogeneous porosity is formed in the interface.

Furthermore, all material parameters of the silver diffusion interface – which have been extensively studied [10] – are superior to conventional solder interfaces as illustrated in table 1.

Table 1: Material parameters for the silver diffusion sinter layer in comparison to a standard solder interface

properties	unit	solder layer SnAg(3)	Ag diffusion sinter layer
melting temperature	°C	221	962
thermal conductivity	W/m/K	70	240
electrical conductivity	MS/m	8	41
layer thickness	µm	~90	~20
CTE	ppm/K	28	19
tensile strength	MPa	30	55

The thermal conductivity is more than a factor of three better than that of a tin-silver solder interface. This improves the transfer of heat together with the reduced layer thickness. The electrical conductivity is enhanced as well. The mechanical characteristics as CTE and tensile strength are favorable for the implementation in power electronic packages.

However, the most important feature of the silver sintering interface is the high melting point of the silver layer. This aspect can best be illustrated by the concept of homologous temperature, which is well known to mechanical engineers. The stability of a material under mechanical stress can be evaluated by comparing the ratio of operational temperature to the melting point temperature on the absolute temperature scale. Fig. 10 shows this ratio for the silver sinter layer in comparison for two solder layers, the widely known SnAg(3) solder and a high melting AuGe(3) solder with a liquidus temperature of 363 °C. Assuming an operation temperature of 150 °C for all three systems, the two solder systems exhibit homologous temperatures above 60%, while the silver sinter technology has a homologous temperature below 40% due to the high melting point of silver. For the long time stability under mechanical stress, homologous temperatures below 40% are considered appropriate, between 40% and 60%

materials are in the so-called creep range and therefore sensitive to strain, whereas above 60% homologous temperature materials are considered 'unable to bear engineering loads'.

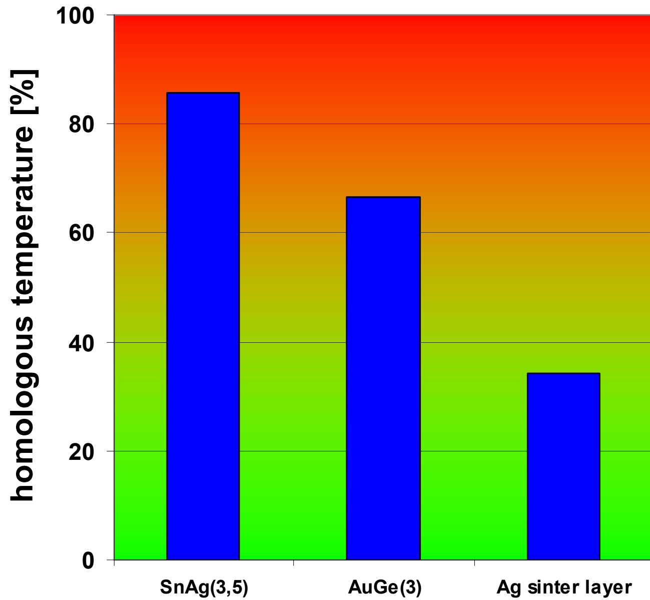

Fig. 10: Homologous temperature for chip interconnection layers assuming an operation temperature of 150°C. The homologous temperature is the ratio of operation temperature to liquidus temperature in K.

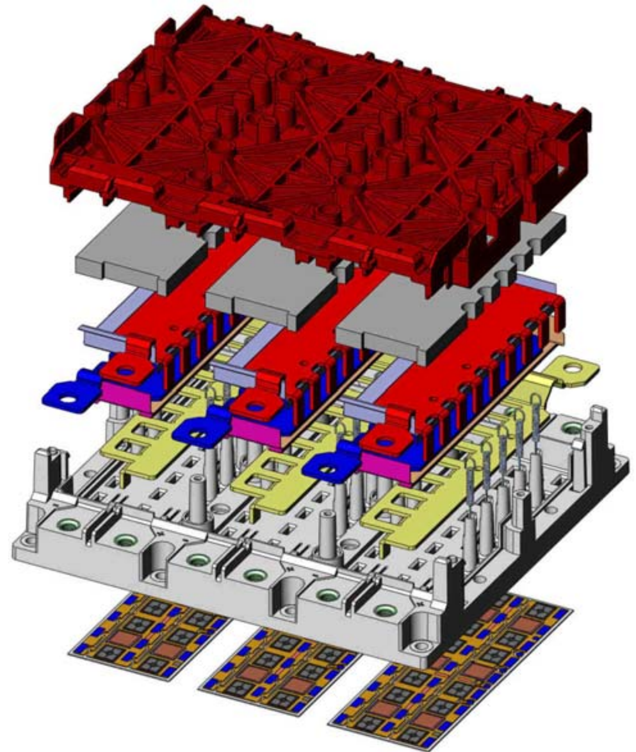

Fig. 11: Explosion view of the first 100% solder-free module, showing the sintered substrates, the multi-contact internal bus bar, the springs for the control and sensor contacts and the pressure system.

An enhanced reliability can be anticipated as a consequence of these favorable characteristics of the sinter technology, because degradation effects as known from solder interfaces are not expected for silver sinter interconnections.

V. The 100% Solder-Free Module

Combining all technologies discussed above in a single module leads to the first modern power module without a single solder interface. Fig. 11 shows an explosion view of the module architecture. Looking at the construction form bottom up, the construction elements can be identified.

On the bottom, the three phase leg power substrates are displayed, carrying two switches formed by six IGBTs and three FWDs each. Each diode is placed between two IGBTs, so that the commutation paths are kept as short as possible. The blue rectangles indicate the landing position of the multi-contact internal bus bars, while the blue circles mark the landing area of the control and sensor contact springs.

The gray housing element aligns the DBC substrates and all electrical connections. The columns for the springs and the mounting bolts (not shown) assure the necessary creepage and clearance distances in the package. A high temperature resistive foil insulates the three elements of the multi-contact internal bus bar systems against each other.

The dark gray pressure foam distributes the pressure homogeneously to all contact positions of the internal bus bar structure. The dark red pressure plate on top – a molded steal structure – transfers the pressure to the whole system.

Engineering samples of the presented module are available in two different versions. The SKiM®63 module combines four IGBTs and two FWDs per switch in a sixpack configuration with a nominal current of 600 A for 600 V blocking voltage. The SKiM®93 package combines six IGBTs and three FWDs per switch to form a 900 A sixpack module for 600 V blocking voltage. Both package sizes are also available for higher blocking voltages.

Reliability tests confirm the expected high reliability of the package. Fig. 12 shows the temperature cycling test result in a two chamber temperature shock test (air to air) with chamber temperatures of -40 °C and +125 °C and dwell times of 90 minutes in each chamber.

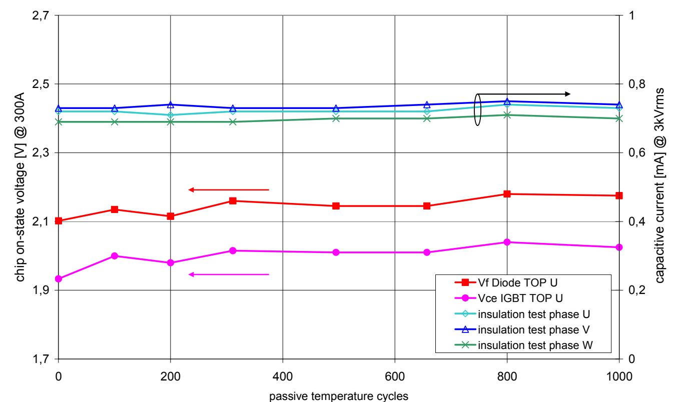

Fig. 12: Temperature shock test result (-40 °C / +125 °C) for a SKiM®63 module, proving stable a contact and insulation for 1000 cycles.

Fig. 12 displays only the typical result for the test, which was performed with a group of six modules; all six modules passed the test. This test result verifies that the presented module architecture is capable of surviving at least 1000 passive temperature cycles, which is far beyond the capability of a classical module design with a copper base plate. An end-of-life temperature cycling test was started with six SKiM® modules to establish a data base for statistical lifetime estimation and to identify failure modes.

The reliability of the SKiM® module during active power cycles was determined by an end-of-life test. The TOP and BOT switch of a single phase leg were connected in series and subjected to a constant DC current of 209 A. During the heating time of approx. 80 s, the chips were heated up to a medium temperature of 140 °C, measured by the $V_{CE}(T)$-method with a small sense current right after the turn-off of the load current. These temperature values were monitored after every cycle for both switches. The forward voltage drop of the two IGBT switches was recorded shortly before the load current turn-off. The results are depicted in Fig. 13.

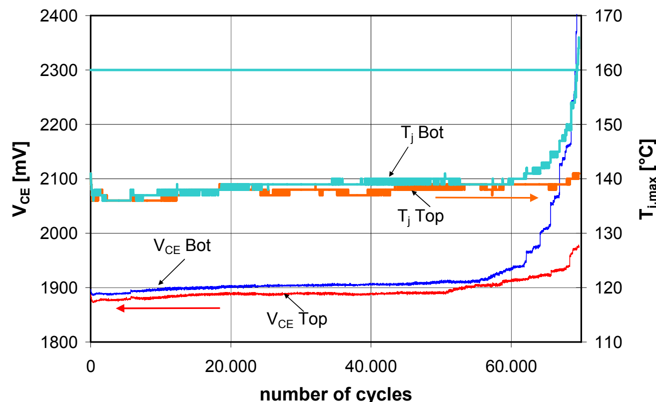

Fig. 13: Power cycling test on a 1200 V SKiM®63 module: the elimination of all solder interfaces increases the lifetime during active power cycles by more than 50%.

For soldered power modules, the number of cycles to failure does not exceed 40,000 cycles under these test conditions, while the SKiM® module survives more than 69,000 cycles until failure. This result confirms that the improvement of the chip to substrate interconnection by the silver diffusion sinter technique leads to an increased lifetime during active power cycling due to the absence of solder degradation effects.

VI. Conclusion

The classical module design with a copper base plate is limited in the capability to withstand passive temperature cycles. The pressure contact system, which eliminates the base plate, can improve the stability under passive temperature cycles considerably.

The current distribution for static and dynamic conditions is efficiently improved by the implementation of internal bus bars with multiple contact positions. This architecture provides an evenly distribution of stress to several paralleled chips and thus increases the system reliability.

The silver diffusion technology enhances the lifetime of power electronic packages by eliminating the degradation of the traditional solder layer between the chip and the substrate.

The reliability test results confirm this expectation and show that the pressure contact technology combined with an internal bus bar structure with multiple contacts and the silver diffusion sinter technology can fulfill the demands of hybrid vehicle traction applications.

References

[1] J.-P. Sommer, T. Licht, H. Berg, K. Appelhoff, B. Michel: Solder Fatigue at High-Power IGBT Modules, Proc. CIPS 2006, Naples, Italy, pp 87-92.

[2] Y. Nishimura, K. Oonishi, A. Morozumi, E. Mochizuki, Y. Takahashi: All lead free IGBT module with excellent reliability, Proc. ISPSD 2005, Santa Barbara, CA, USA, pp 79-82.

[3] J.-P. Sommer, R. Bayerer, R. Tschirbs, B. Michel: Base Plate Shape Optimisation for High-Power IGBT Modules, Proc. CIPS 2008, Nuremberg, Germany, ETG-Fachbericht 111, pp 323-326.

[4] M.H. Poech, R. Eisele: A Modelling Approach to Assess the Creep Behaviour of Large-Area Solder Joints, Microelectronics Reliability 40 (2000), pp. 1653-1658.

[5] U. Scheuermann, J. Lutz: High voltage power module with extended reliability, Proc. EPE99, Lausanne, CD-ROM (1999).

[6] G. Lefranc, T. Licht, H.J. Schultz, R. Beinert, G. Mitic: Reliability Testing of High-Power Multi-Chip IGBT Modules, Microelectronics Reliability 40 (2000), pp 1659-1663.

[7] U. Scheuermann: Power module design for HV-IGBTs with extended reliability, Proc. PCIM, PC1.4, 49-54, Nürnberg, 1999.

[8] U. Scheuermann: Advanced Power Modules with AlN-substrats – extending current capability and lifetime, Proc. PCIM 2003, Nuremberg, PE 12.5, pp 309-314.

[9] U. Scheuermann, P. Wiedl: Low Temperature Joining Technology – a High Reliability Alternative to Solder Contacts, Workshop on Metal Ceramic Composites for Functional Applications, 181-192, Wien, 1997

[10] C. Mertens: Die Niedertemperatur-Verbindungstechnik in der Leistungselektronik, Ph.D. Thesis, 2004, Fortschritt-Berichte VDI, Reihe 21, Nr. 365