

600V SOI Gate Drive HVIC for Medium Power Applications Operating up to 200°C

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Abstract

The design, functionality and measurements of a fully integrated 600V SOI gate drive IC are presented. The seven-channel HVIC is aimed at three-phase systems for low power and medium power applications. Dielectric device isolation and detailed circuit design ensure operation up to a temperature of 200°C. Robust signal processing has been given highest attention at all design stages. A dedicated signal reconstruction topology is presented to provide maximum immunity against parasitic coupling from the power plane. The measurements confirming the safe operation of the IC are given.

Introduction

IPM solutions for medium power applications (600V, <50A) are aimed at high volume markets, where system costs and geometric size per function are the most relevant parameters. IC-based designs are thus replacing conventional hybrid IGBT and MOS drivers [1] [2] [3] [4].

Due to the high production numbers, fully integrated solutions are feasible which combine both driving circuitry and power bridges on a single die [5]. Widely accepted gate drive ICs rely on conventional junction isolation to achieve 600V blocking voltage and to shield the high side from the offset voltage [6] [7]. Though the market has shown considerable interest in these HVICs, the junction isolation has certain fundamental drawbacks. Negative transient voltages at the driver output can trigger internal parasitic structures, leading to latch-up. The problem can be somewhat alleviated by minority carrier suppression structures [8] [9] [10] but it cannot be resolved completely. Also, increasing pn leakage currents typically limit the operation temperature to 150°C.

600V SOI Technology

A high voltage SOI platform, on the other hand, can provide complete latch-up immunity since all active devices are dielectrically insulated. This enables the operational tempera-

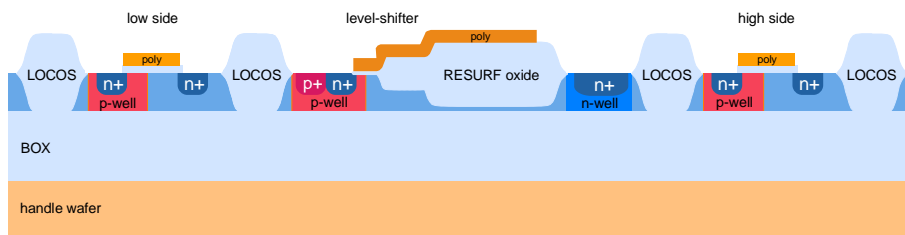


Fig.1 Schematic cross section of the foundry HV SOI technology [11] [12]

ture range to be considerably extended.

The chip was made with a 600V SOI foundry process [11] [12]. Fig.1 shows a schematic cross-section of the 600V SOI technology. The key to the high breakdown voltages is the selective layer thinning in high voltage areas [13] [14]. Figs. 2 and 3 illustrate the operation principle.

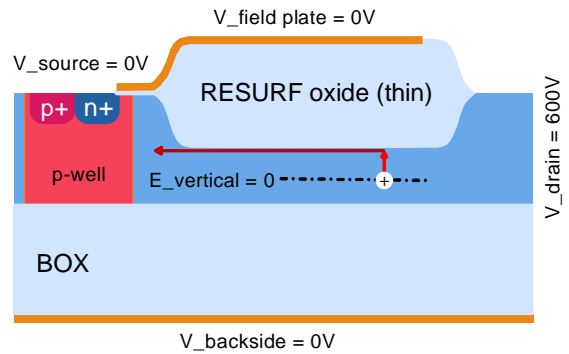


Fig.2 Vertical and lateral avalanche path in thick active silicon

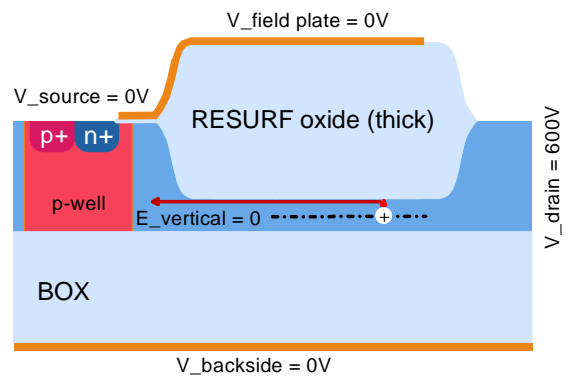


Fig.3 Vertical and lateral avalanche path in thin active silicon

While the lateral ionization paths are the same in both cases, the carrier multiplication due to vertical field components is drastically reduced in Fig.3 because of the reduced vertical avalanche path length.

One way of determining the breakdown voltage limit of the structure in Figs. 2 and 3, is to calculate the worst-case avalanche paths along the vertical and lateral device dimensions. This is not an exact solution because of the two-dimensional nature of the problem. For integrated level-shifter transistors such as are used in gate drive ICs, the lateral field components can be adjusted by choosing the appropriate drift zone length. This is not a design constraint, since the current levels of the level-

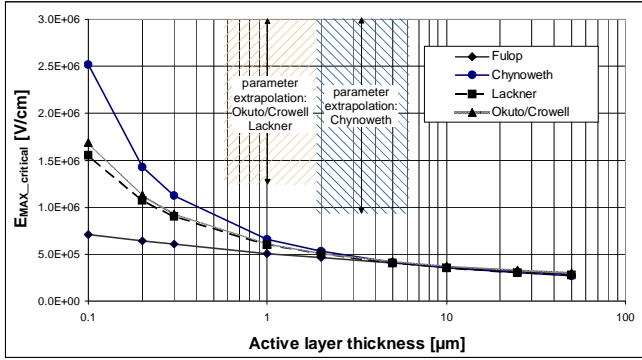


Fig. 4 Comparison of critical peak field values

shifter are low. Therefore, it is the vertical component which limits the maximum breakdown voltage. The well-known Chynoweth relation [15] and its parameterization according to van Overstraeten and de Man [16] are commonly employed to model avalanche multiplication in drift zones of power devices. However, in the case of high fields and especially over short path lengths, more physically motivated models such as the ones after Okuto/Crowell [17] [18] or Lackner [19] give more consistent predictions. It should be noted, that most analytical formulations of the problem are based on the polynomic Fulop model [20], which must not be used in this range of field strengths. Fig. 4 gives a comparison of the maximum sustainable fields according to different models. The diagram refers to a one-dimensional vertical field with triangular shape as found in the structures of Figs. 2 and 3. The field drops from its peak value E_{MAX} at the silicon/oxide interface to zero towards the middle of the active layer. Thus, the ionization path length is half the thickness of the active layer. The value $E_{MAX_critical}$ denotes the peak field value where the avalanche integral approaches 1. The models after Okuto / Crowell and Lackner better represent device physics. The mutual consistency of their results supports the assumption, that these models should replace the Chynoweth model for the given case.

System and HVIC design

Fig. 5 shows a block diagram of the target power conversion system. The topological blocks to be integrated into a gate drive HVIC are marked. Only two of the seven channels are shown. Depending on the field of application, additional blocks such as the V_{CE} detection diodes can easily be integrated as well. The IC block diagram is given in Fig. 6. Input interfaces (IIF) implement logic thresholds for direct connection to 5V or 3.3V micro-controllers. An interlock time is usually implemented in the external drive controller pattern and the user can activate a hardware interlock in the gate driver. Both methods minimize cross-currents in the external power bridge. Logic and error management generate the appropriate internal signals. These take into account not only under-voltage

lockout (UVLO) as derived from a bandgap-stabilized reference but also external analog sensor signals such as shunt current monitoring.

The branch delay times of the six main channels TOP/BOT1-3 are delay-matched to ensure synchronized switching. A 7th channel is implemented at the low side to support power factor correction schemes or to be used as a brake chopper. Three 600V level-shifters transfer the signals to the fully isolated high sides, where the differential transmission signals are filtered and reconstructed. The signals are driven at the chip output by a CMOS stage of the 500mA sink / 250mA source type. The driver operates at 15V. High side supply is implemented by a bootstrap circuit with integrated HV diodes. Fig. 7 is a microphotograph of the chip (an evaluation version carrying additional test pins).

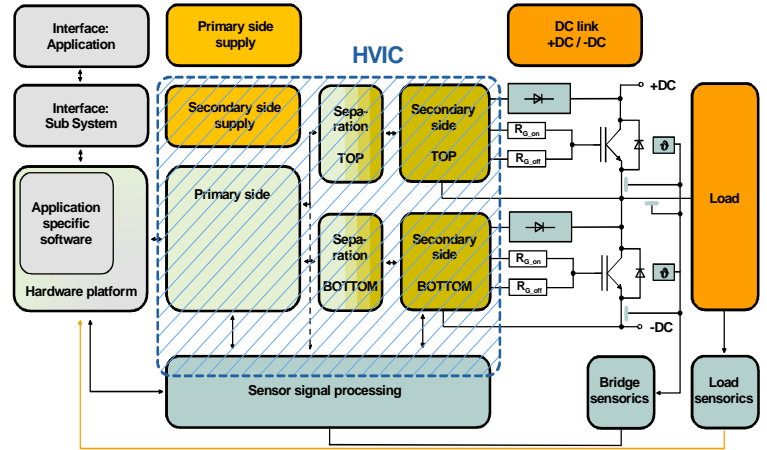


Fig. 5 Integration area covered by the HVIC (2 of 7 channels)

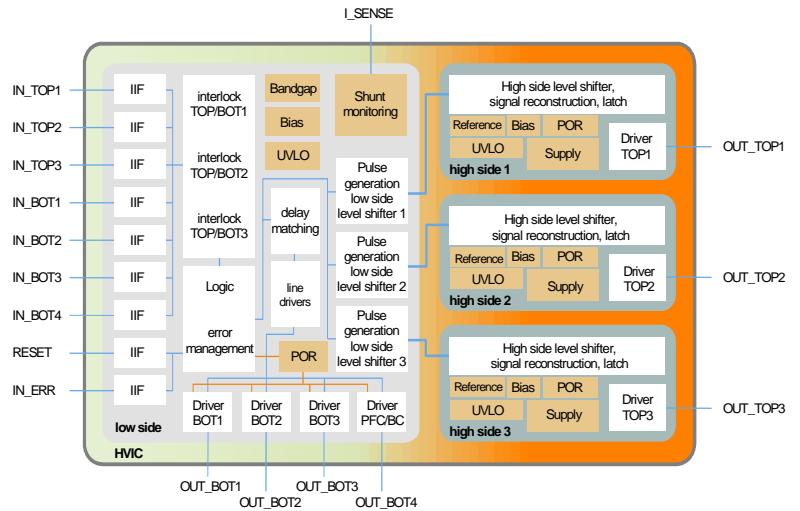


Fig. 6 Block diagram: seven-pack gate drive HVIC

Level-shifter design

The single most important internal function of the gate drive IC is to transmit signals from the controlling low side to the three high sides. The signal reconstruction scheme at the high side, in particular, where the transmitted raw pulses are interpreted and converted into valid control patterns, is of fundamental importance. The reconstruction scheme has to separate signals from any voltage or current disturbances

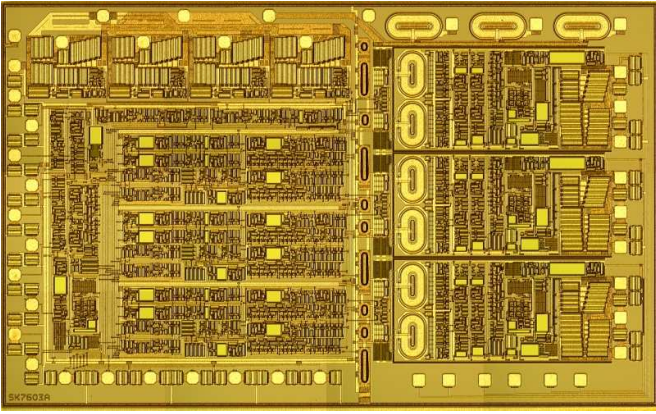


Fig. 7 Chip photograph of the seven-pack gate drive HVIC (chip size approximately 12mm²)

which couple back into the IC from the electromagnetically polluted system environment.

The raw signal transmission uses two conventional cascode switch configurations as shown in Fig. 8. The 600V device isolates the low side from the high side. As soon as the transistor M_1 opens, a cross-current I flows from the high side supply v_{dd_hs} to low side ground (gnd_ls). The current is limited in M_1 by source feedback over R_{lim} . The voltage drop across R_{hs} is the high side raw signal (V_{OUT}).

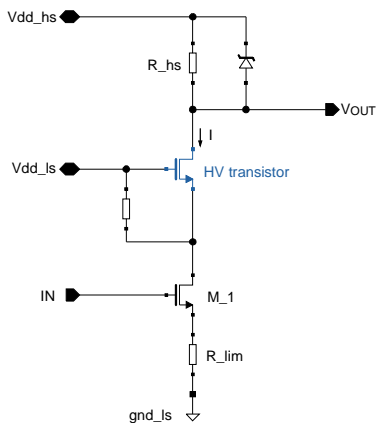


Fig. 8 Level-shifter cell (two per channel for differential transmission)

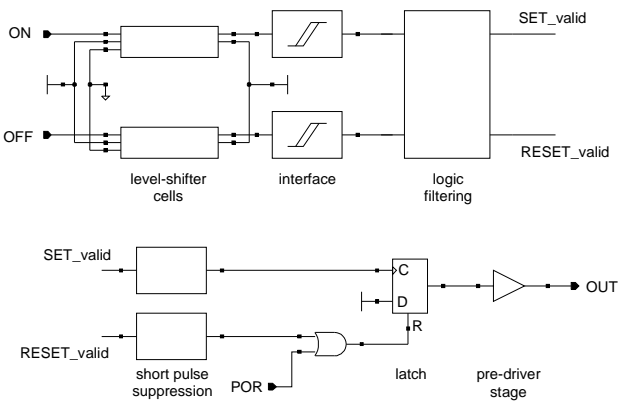


Fig. 9 Signal reconstruction topology

A differential scheme is necessary because of common mode currents flowing through the cell during every dv/dt event between low side and high side. These events are caused by normal switching of the respective channel or by parasitic

coupling between channels. The signal reconstruction which has been developed and is shown in Fig. 9 relies on individual recognition and processing of the two raw signals rather than a conventional conversion, from differential to single-ended, using latching stages.

The high robustness obtained for the level-shifter is due to the combination of three factors: wide signal swings with interface hysteresis; simple, yet effective logic filtering of common mode signals; and short pulse suppression. The experimental results presented later are the proof of this. The signal POR (power on reset) in Fig. 9 ensures the power-up of the latch that is storing the drive information.

Measurements

All high voltage measurements were taken with the gate drive IC operating on a SEMIKRON MiniSKiiP II Module (six-pack, 600V / 10A trench IGBT with CAL free-wheeling diode). The module outputs are connected to individual resistive-inductive loads. Fig. 10 shows a photograph of the measurement setup.

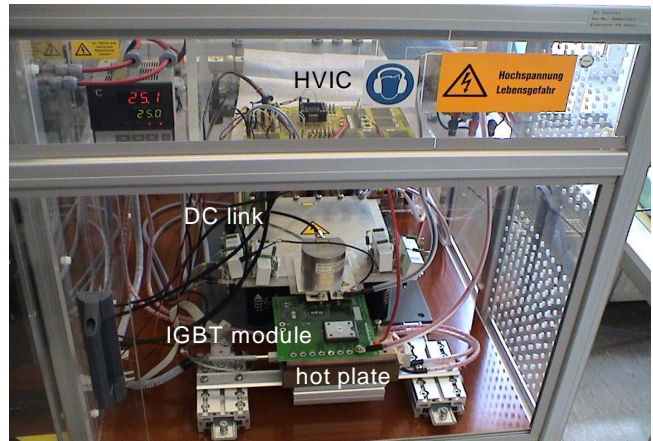


Fig. 10 High voltage measurement setup

A. Normal operation

Fig.11 shows simultaneous operation of two TOP channels at 400V DC link voltage. No signal interference was observed between the neighboring high sides of the gate driver. The channels can have arbitrary mutual timing.

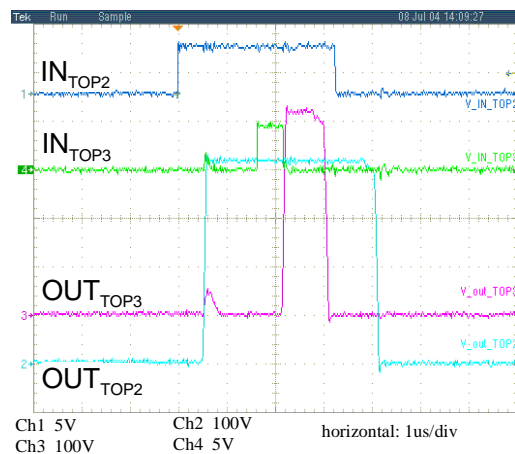


Fig. 11 Independent switching of two TOP channels at 400V DC link voltage

B. Robustness of operation

Several potentially hazardous situations that exceed the limits of regular operation have been tested. Fig. 12 shows measurements at increased DC link voltage of 500V. The most critical timing is shown where a phase of high dv/dt at the output of channel TOP3 coincides with a signal transition at the input of channel TOP2. Even at 3.3V input level the internal signal filtering safely recognizes the transition. Another measurement is shown in Fig. 13 of the IGBT turning on into a hard short circuit and generating harsh current and voltage transients. Internal shunt monitoring produces a reaction as soon as the current rises above the short circuit threshold. A local error signal I_ERR tracks the fault. The global error signal ERR_OUT is generated and sent back to the micro-controller and the IGBTs are turned off.

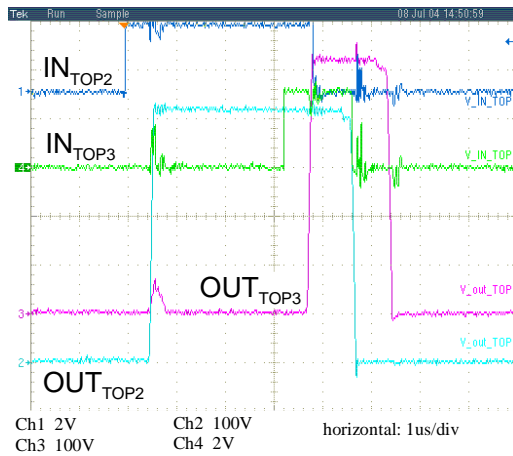


Fig. 12 Safe 3.3V signal recognition at $V_{DC}=500V$

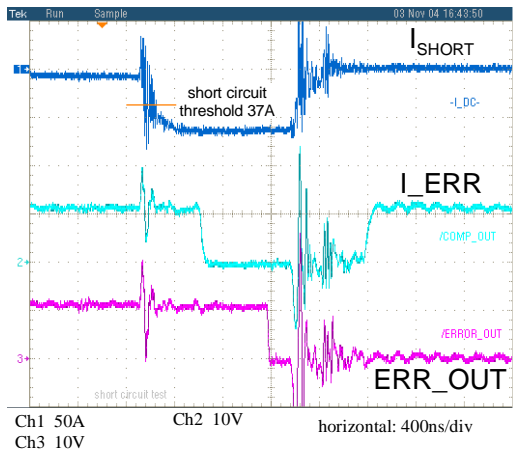


Fig. 13 Short circuit management

C. High temperature operation

While the IC has been standard-tested at ambient temperatures between $-40^{\circ}C$ and $105^{\circ}C$, additional measurements have been taken at core temperatures up to $193^{\circ}C$ (Fig. 14). This correlates with driver stage temperatures above $200^{\circ}C$. All the outputs were switched at a capacitive load of 2nF. The core temperature was measured using an internal diode, that had been temperature calibrated in a climate chamber. The IC retained full functionality at all temperatures. Defining the maximum temperature for continuous operation

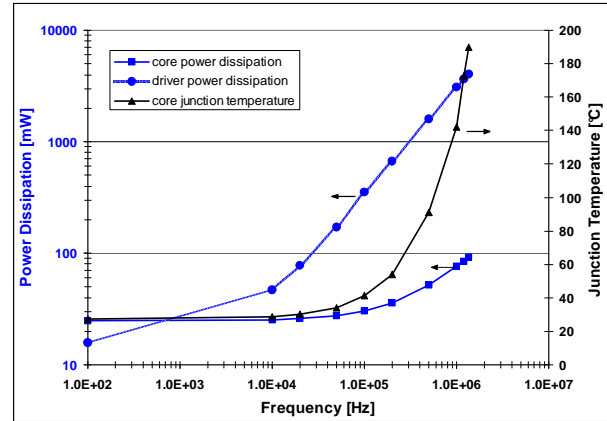


Fig. 14 Current consumption and core temperature measurement (core: 4 low sides + 3 high sides; drivers stages excluded)

requires that the lifetime of the on-chip metal interconnects must be taken into account. For the measurement given in Fig. 14, the employed TQFP package was limiting the temperature range. Even at switching frequencies above 1MHz, the IC core dissipates less than 100mW. Thus, high operation robustness has been achieved with low current consumption.

Conclusion

High voltage SOI technologies are available that allow monolithic integration of a seven-pack gate drive HVIC for 600V systems. In determining the maximum sustainable voltage, advanced avalanche models are to be preferred over the common Chynoweth relation. Specific work on signal integrity and robustness against coupling from the power environment has led to safe HVIC operation under all conditions tested: low voltage input, high output dv/dt , short circuit and driver stage temperatures higher than $200^{\circ}C$.

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References

- [1] Data sheet, SPM™ DIP-SPM, Fairchild Semiconductor, 2003
- [2] Data sheet, IRAMS06UP60A, International Rectifier, 2003
- [3] Data sheet, DIP-IPM, Mitsubishi Electric, 2002
- [4] Sung-il Yong, Bum-Seok Suh et al., Power Systems Design Europe, Issue September 2004, pp. 12-17
- [5] H. Akiyama et al., Proceedings ISPSD 2004, pp. 375-378
- [6] Toshio Takahashi, Proceedings CIPS 2000, pp. 73-81
- [7] Data sheet, L6384, STMicroelectronics, 2000
- [8] S. Gupta et al., IEEE Electron Device Letters, Vol. 22, No. 12, 2001
- [9] J.P. Laine, O. Gonnard, G. Charitat et al., Proc. ISPSD 2002, pp. 273-276
- [10] V. Parthasarathy, V. Khemka, et al., Proc. ISPSD 2004, pp. 427-430
- [11] T. Letavic, E. Arnold, M. Simpson et al., Proc. ISPSD 1997, pp. 49-52
- [12] T. Letavic, M. Simpson, E. Arnold et al., Proc ISPSD 1999, pp. 325-328
- [13] S. Merchant et al., Proceedings ISPSD 1991, pp. 31-34
- [14] S. Merchant et al., Proceedings ISPSD 1993, S. 124 – 128
- [15] A.G. Chynoweth, Phys. Rev., Vol. 109, Number 5, S. 1537-1540, 1958
- [16] R. van Overstraeten et al., Solid State Elec., Vol. 13, S. 583 – 608, 1970
- [17] Y. Okuto, C. R. Crowell, Phys. Rev. B., 6(8), S. 3076 – 3081, 1972
- [18] Y. Okuto, C. R. Crowell, Phys. Rev. B., 10(10), S. 4284 – 4296, 1974
- [19] T. Lackner, Solid-State Electronics, Vol. 34, S. 33 – 42, 1991
- [20] W. Fulop, Solid-State Electronics, Vol. 10, S. 39 – 43, 1967