

600V SOI Gate Driver IC with Advanced Level Shifter Concepts for Medium and High Power Applications

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Keywords

«High voltage IC's», «Power integrated circuit», «Smart Power», «SOI-device», «System integration»

Abstract

An advanced level shifter topology allows any desired reference voltage drop between the primary side and the secondary sides of a high voltage IC (HVIC), including negative voltages caused by parasitic elements. This makes the HVICs suitable for medium and high power applications. For integration into latch-up free SOI technology the advanced level shifter topology is preferable. The capabilities of the level shifters are demonstrated in an experimental 7-channel 600V gate driver IC. It is demonstrated that the circuit remains operational for negative reference voltages down to -45V (bottom channel) and -20V (top channel) respectively.

Introduction

Intelligent Power modules (IPM) with fully integrated solutions which combine both driving circuitry and power bridges on a single die [1] or at least with implemented IC-based driver [2] replacing conventional hybrid IGBT and MOS drivers are restricted to low power applications (600V, 1200V, < 30A). Gate drive ICs, widely accepted, rely on conventional junction isolation to achieve 600V (1200V) blocking voltage and to shield the high side from the offset voltage [3]. Though the market has shown considerable interest in these HVICs, the junction isolation has still had certain fundamental drawbacks. Negative transient voltages at the driver output can trigger internal parasitic structures, leading to latch-up. The problem can be somewhat alleviated by minority carrier suppression structures [4] [5] [6] but it cannot be resolved completely. Also, the operation temperature is typically limited to 150°C because of increasing pn leakage currents.

A high voltage SOI-CMOS (600V) platform technology [7] [8] can provide complete latch-up immunity since all active devices are dielectrically insulated (Fig. 1). The regular CMOS circuits of the low side and the high side are based on quasi-bulk transistors in fully isolated silicon islands, so that the operational temperature range can be considerably extended, up to 200°C [9].

Reference voltage aspects in integrated gate drivers

Figure 2 shows a typical half-bridge driver circuit consisting of MOS power switches and an integrated gate driver IC. Also shown are some typical parasitic elements (inductances) in the power

plane as well as in the gate drive. Even in low current applications and, yet more, in medium and high current applications, where high currents or high dI/dt are switched, positive and negative voltage peaks can occur on the parasitic elements. An associated resistive voltage drop in the power plane is also possible.

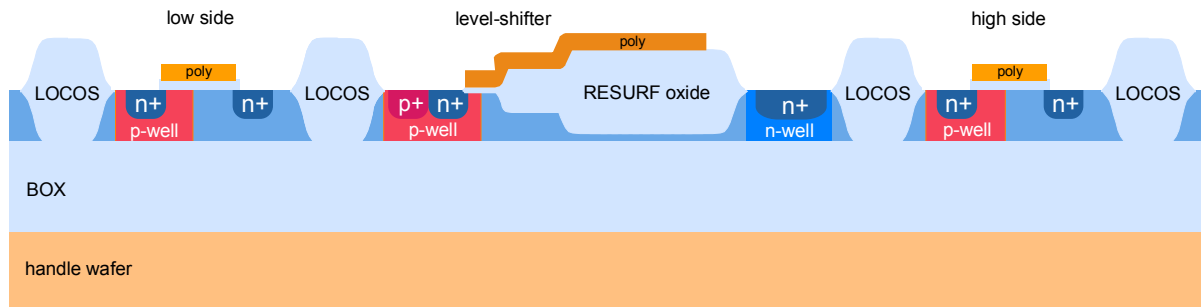


Fig. 1: Schematic cross section of the foundry HVSOI technology [7] [8]

In a typical set up with integrated gate drivers as shown in Fig. 2, the reference point of the bottom (BOT) driver (V_{sL}) is connected internally to the primary side reference potential (GND). In this case positive or negative voltage shifts caused by the parasitic elements have an impact on the gate-source voltage of the BOT switch, which, in a worst case scenario, could lead to defective switching behaviour.

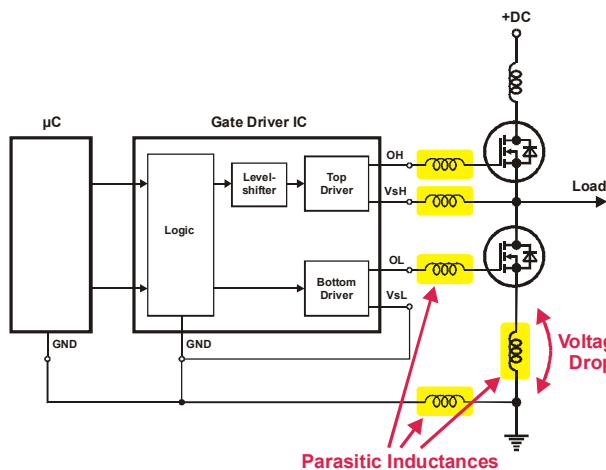


Fig. 2: Effect of parasitic elements on a gate driver circuit

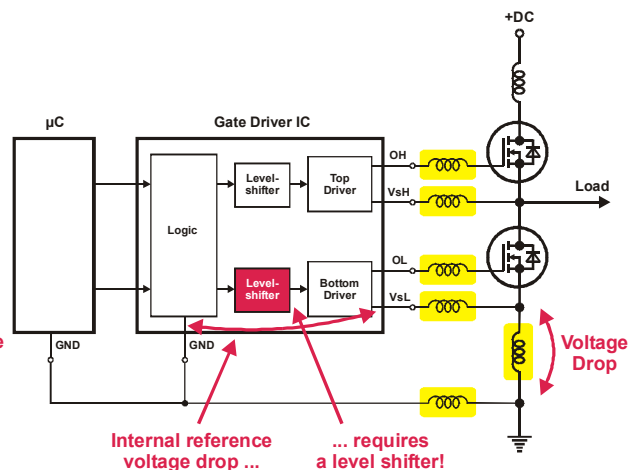


Fig. 3: Connection of the BOT driver to a more advantageous reference potential

A more favourable solution to produce a stable gate-source voltage at the BOT switch is shown in Fig. 3, where V_{sL} is connected directly to the source of the BOT switch. In this case, the influence of parasitic components in the power plane is strongly reduced. Additionally, the effect of the remaining parasitic inductances in the gate circuit can be eliminated by pairing the driver output wires (O) and driver return wires (V_s).

Another typical circuit for low or medium power applications, often used in IPMs, is shown in Fig. 4. There is a protection circuit with a shunt resistor in the ground plane to shut down the driver in the event of overcurrent. The shunt resistor also causes a load-dependent voltage shift, which acts as an additional parasitic element in the power plane.

The voltage drop over parasitic elements is, however, not eliminated, but occurs in the IC in this configuration (Fig. 3), necessitating the integration of a level shifter into the BOT channel. Because it is possible for the polarity of this voltage to be positive as well as negative, a level shifter with bipolar characteristics is desirable. The restrictions concerning negative voltages in junction-isolated HVICs

commonly allows only a few volts (typically -5V) below ground potential. The design goal of an advanced level shifter is the significant extension of the range of the operational voltage shift.

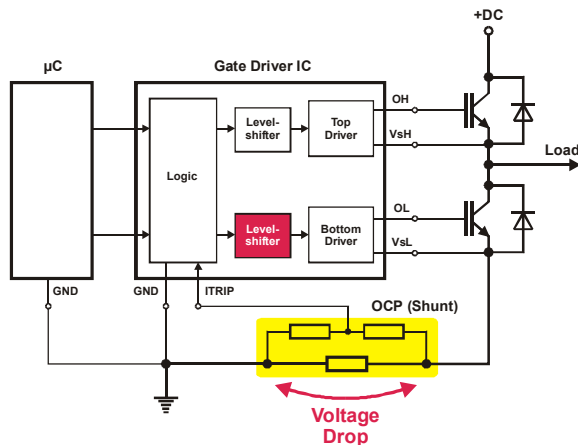


Fig. 4: Over current protection (OCP) with shunt resistor

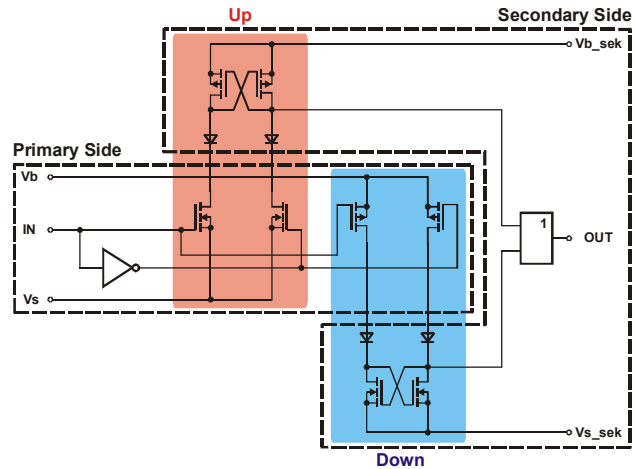


Fig. 5: Circuit principle with up-/down- level shifter for the BOT channel

The advanced level shifter concept

BOT channel level shifter

The circuit principle of the BOT channel level shifter is shown in Fig. 5. It consists of two independent transmission paths, an up-level shifter and a complementary down-level shifter. The configuration is that of a conventional static CMOS level shifter with additional diodes in each path. Both the up- and the down-level shifters use two cross coupled parallel branches with the function of a latch. Hence there are no cross currents under static voltage conditions. Because of the full dielectric isolation of each device, the circuit itself is latch-up free. For this reason and also that of the weak back gate effect of the used SOI technology every circuit part can carry any desired potential. The maximum allowable offset voltage is only limited by the breakdown voltage of the level shifter transistors.

Depending on the polarity of the offset voltage between the primary and the secondary side ($V_{\text{offset}} = V_{\text{vs_sek}} - V_s$) the up-level shifter ($V_{\text{offset}} \geq 0V$) or the down-level shifter ($V_{\text{offset}} \leq 0V$) transmits the applied input signal from the primary to the secondary side. The inactive path is blocked by the reverse-biased diodes. To reconstruct the signal on the secondary side, a simple logic disjunction may be used.

TOP channel level shifter

The circuit principle of the TOP channel level shifter is shown in Fig. 6. As in the case of the BOT channel, the level shifter consists of two complementary parts: the high voltage up-level shifter and the low voltage down-level shifter. Because there are no p-MOS devices available with a breakdown voltage extending to 600V, a pulsed signal transmission requiring simply a high-voltage n-DMOS and high-voltage diodes, to block the high reverse voltage in the down-level shifter, is used. Pulsed transmission is applied to minimize the cross current and power consumption but requires more complex signal generation and reconstruction in comparison to the BOT channel. The differential transmission with two branches per level shifter, a robust signal processing and reconstruction on the secondary side provide maximum immunity against parasitic coupling from the power plane.

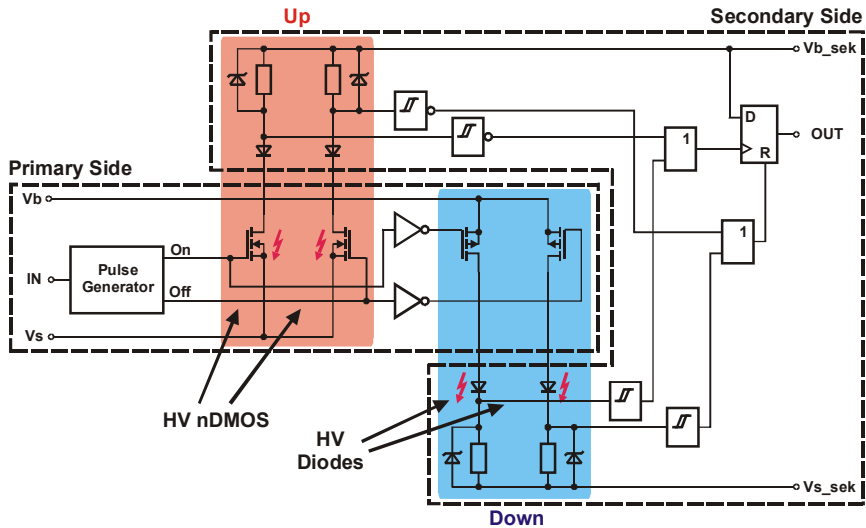


Fig. 6: Circuit principle with up-/down- level shifter for the TOP channel

7-channel gate driver test circuit

Figure 7 shows the block circuit diagram of an experimental 7-channel gate driver IC. It contains all the functionality needed for a three-phase power system. A fourth independent BOT channel is implemented for PFC or brake chopper applications. The inputs are compatible to TTL and 3.3V CMOS-logic. The driver outputs provide approximately 500mA / 660mA (source / sink) peak output current at 15V supply voltage and room temperature, which will suffice to drive IGBTs directly in low and medium power applications up to several 10A. The supply voltage may vary from 10V to 17V without loss of function. The typical signal propagation delay is about 300ns. The integrated error processing includes undervoltage lockout (UVLO), power on reset (POR), overcurrent monitoring (ITRIP) and external error signals. Each TOP channel has a separate bandgap reference and a UVLO circuit in order to monitor the high side operational voltage. This feature may be important if the TOP channels are powered by a bootstrap circuit. Figure 8 is a chip photograph of the IC. Since this is a test circuit, the layout has not yet been fully optimized.

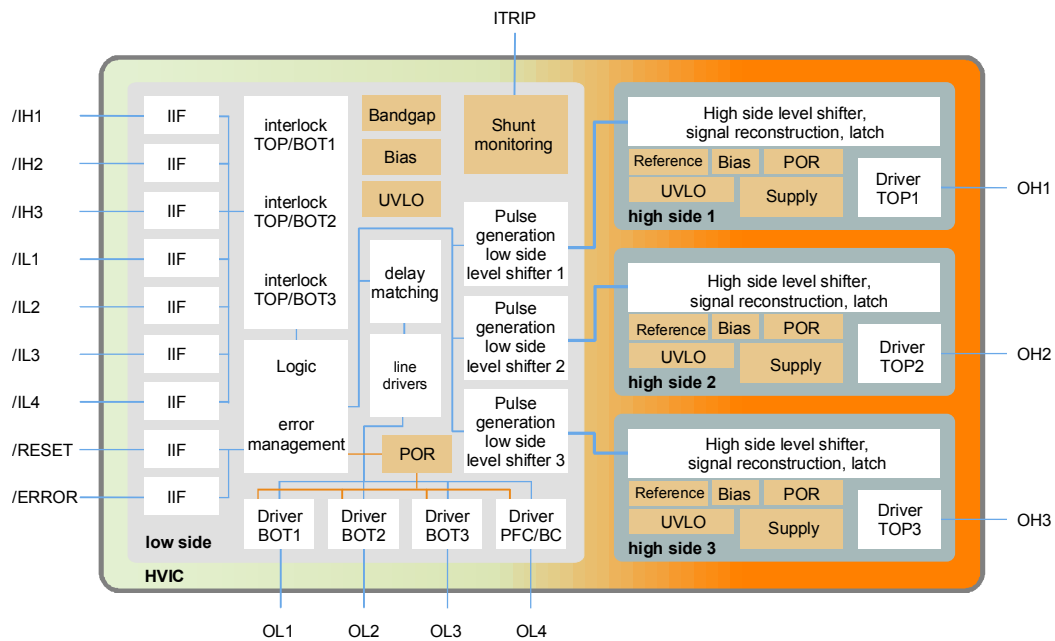


Fig. 7: Block circuit diagram of the 7-channel gate driver IC

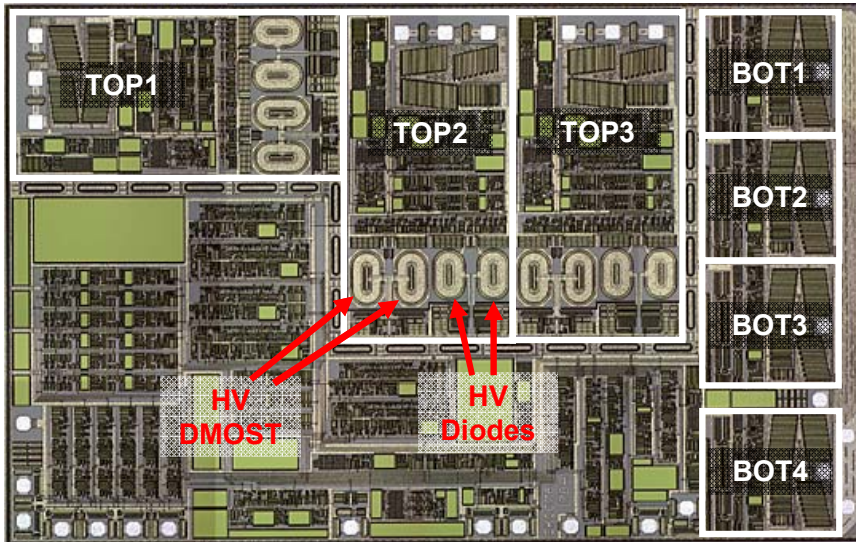


Fig. 8: Chip photograph of the 7-channel gate driver test circuit, size: approx. 4,9x3.1mm²

Measurement results

The typical input and the output waveforms of a TOP and a BOT channel for different static offset voltages are shown in Figures 9 and 10 respectively. For these measurements, two independent, i.e. non-interlocking, channels (TOP3/BOT1) are controlled by the same input signal: it is important to note that all input signals of the test circuit are inverted (low active). The fact that the signal transmission is correct for a positive offset voltage (Fig. 9) as well as for a negative offset voltage (Fig. 10) becomes clear. The propagation delay mismatch between the TOP and BOT channels stays below 20ns for all offset voltages. The minimum negative static offset voltage level is determined by a protective circuit within the down-level shifter of the TOP channel, protecting the TOP channel down-level shifter from large voltage peaks during load switching. Signal transmission for offset voltages below -20V is thus prevented. In fact, as demonstrated below (Fig. 14), the BOT channel level shifter is able to handle much greater negative offset voltages without malfunction or destruction.

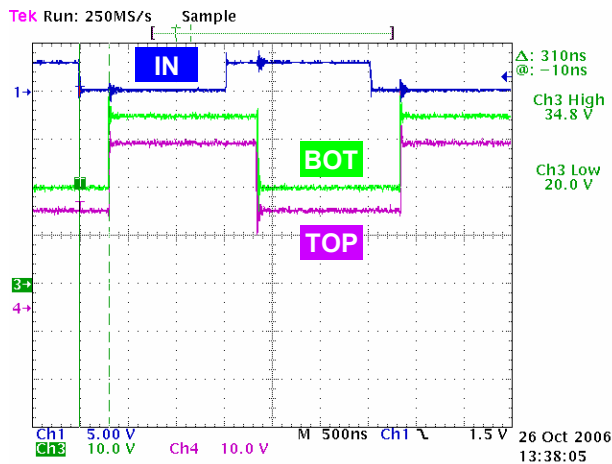


Fig. 9: Typical signal pattern at +20V offset voltage

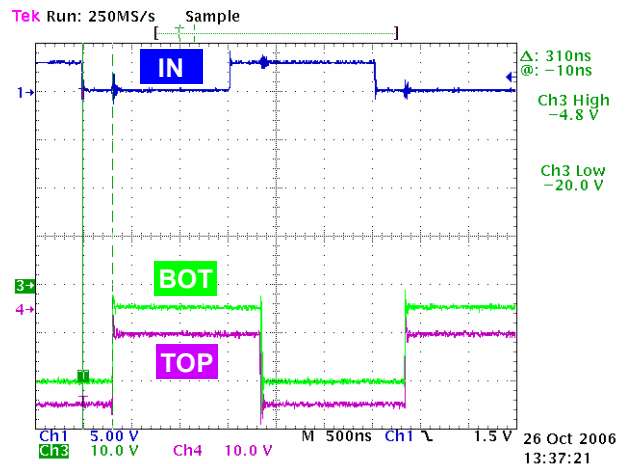


Fig. 10: Typical signal pattern at -20V offset voltage

Figure 11 demonstrates the correct behaviour of the driver under very noisy offset voltage conditions. The *Offset* signal, driven by a noise generator, is the voltage between VsL and/or VsH, and GND (see Fig. 2). Also shown are the (noisy) output signals *BOT* and *TOP* referenced to GND, and (without noise) those related to VsL and VsH respectively. There is stable signal transmission for both channels, indicating a large interference resistance.

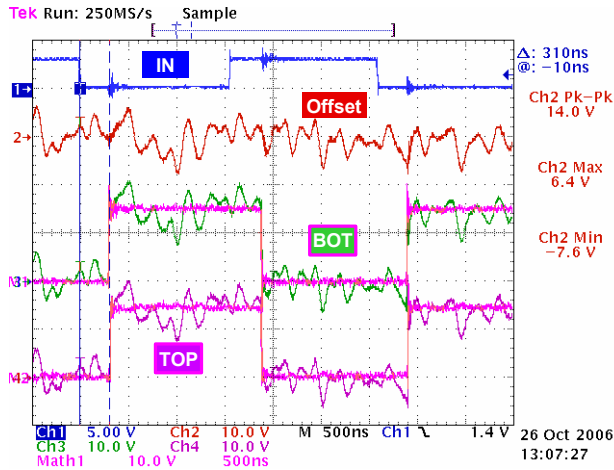


Fig. 11: Typical signal pattern with noisy offset voltage

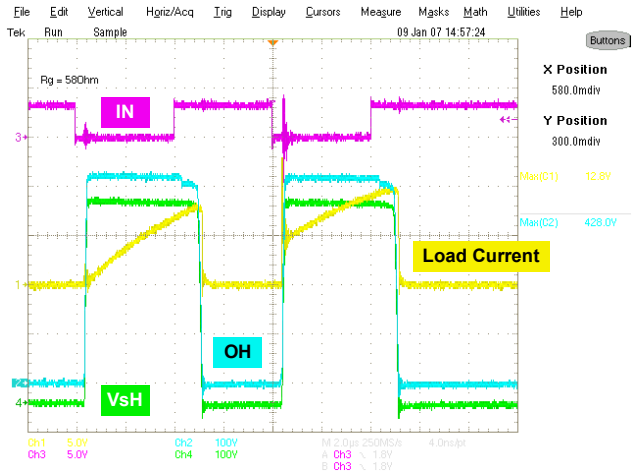


Fig. 12: TOP channel normal operation at 400V DC link voltage (double pulse measurement)

The normal operation of one TOP channel under high voltage conditions is shown in Fig. 12. To check the EMI resistance of the IC, a double-pulse measurement with a directly driven 600V/30A IGBT at 400V DC link voltage into an inductive-resistive load is performed. The most critical aspect of EMI is the rising edge of the second pulse where much noise is generated. Another interesting question is whether the TOP channel down-level shifter might cause a malfunction at large dV/dt . However, the measurement shows stable functioning under all operational conditions. There is neither unwanted switching when the input signal is disturbed by the second pulse rising edge nor any malfunction caused by the down-level shifter.

The circuit shown in Fig. 13 is employed to test the transient behaviour of the down-level shifters. A transient negative offset voltage is generated by turning off an n-MOSFET (T) with an inductive load (L) in the source branch. The n-MOSFET is driven by the gate driver output. The minimum negative voltage is limited by a zener diode (D) in order to not exceed the operational conditions. The secondary side operational voltage (V_{bL} and V_{bH}) is fed by a resistor (R). In conjunction with the bypass capacitor (C), this allows a floating supply to the secondary side for short pulses. The test sequence is as follows. A first short pulse (*on*) stores energy in the inductor. When T is turned off (*off*) the commutation current flows throughout the zener diode causing a negative voltage at the secondary supply return (V_{sL} and V_{sH}). A second pulse (*on*) is applied shortly after the first pulse while the secondary side reference voltage is at its minimum. The driver output should be certain to turn on in this case.

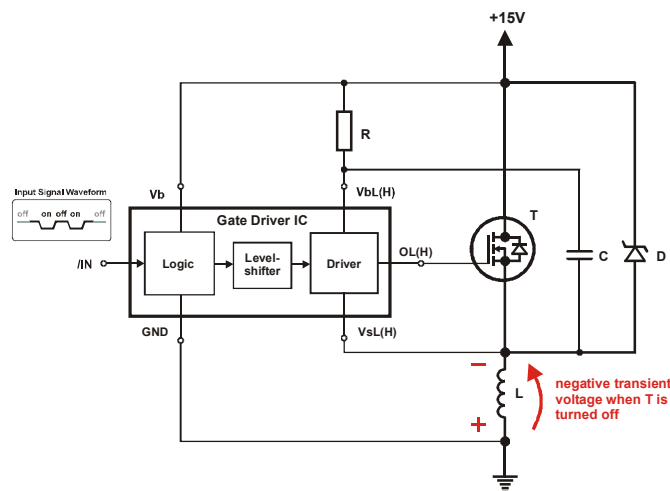


Fig. 13: Negative transient offset voltage test circuit

Figure 14 shows the negative transient offset measurement for the BOT channel. The offset voltage is limited to -45V due to the breakdown voltage of the level shifter transistors ($BV_{DS} > 50\text{V}$). Under this condition, the circuit remains fully functional: no latch-up occurs. The second pulse is certain to transmit without additional delay. The -45V would appear to be the largest negative operational offset voltage reported yet for a CMOS gate driver HVIC.

The negative transient offset measurement in the case of the TOP channel is shown in Fig. 15. The offset voltage is limited to -20V due to a protective circuit in the TOP level shifter as mentioned above. The results are similar to those for the BOT channel measurement.

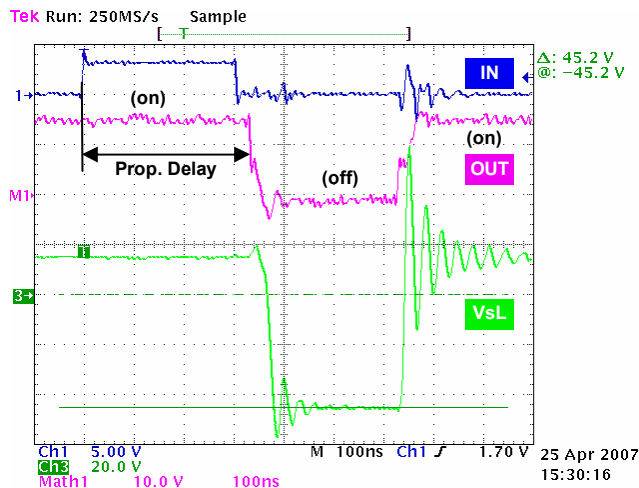


Fig. 14: BOT channel negative transient offset voltage

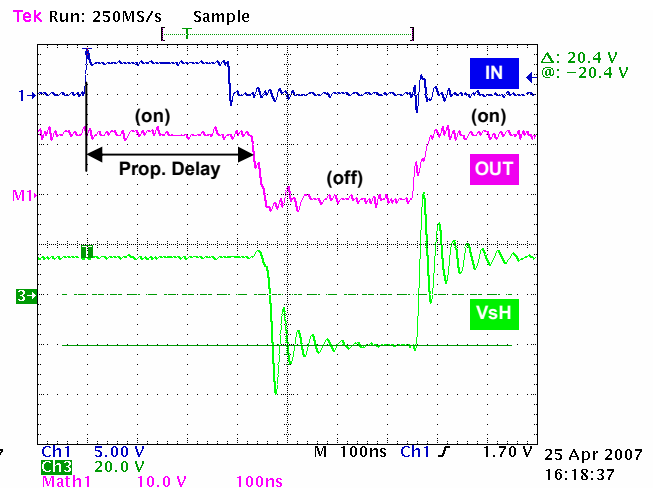


Fig. 15: TOP channel negative transient offset voltage

Conclusion

We have developed an advanced level shifter topology for integrated gate drivers. A down-level shifter for each channel allows the presence of negative secondary offset voltages. The gate driver remains fully operational for any applied offset voltage, providing flexibility in the design of a power system and possibly extending the use of HVICs to medium and high power applications. The advanced level shifter topology has been tested in an experimental 7-channel 600V gate driver IC. The measurements show latch-up free operation for any desired offset voltage down to -45V (BOT) and -20V (TOP).

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