Influence of DC-Link Inductance on Switching Performance and Power Losses

1. Introduction

The power dissipation $E_{on}/E_{off}$ of the IGBT and $E_{rr}$ of the diode specified in the data sheets are measured under certain parameters. In addition to parameters such as the DC-Link voltage, current, junction temperature, gate resistance and gate-emitter voltage, the losses also depend on the inductance of the commutation loop. Figure 1 shows the three main inductive parameters of the commutation loop as centred elements using a simplified inductive equivalent circuit diagram. The power module shown as a half bridge has an internal module inductance $L_{CE}$. The DC-Link inductance $L_s$ consists of the internal inductance of the DC-Link capacitors $L_{Cap}$ and the busbar inductance $L_{busbar}$. These two quantities are determined by the type of capacitor, the number of capacitors connected in series and in parallel and the busbar design. This inevitably leads to different DC-Link inductances $L_s$ used at SEMIKRON and at the customer. The aim of this Application Note is to illustrate the influence of the DC-Link inductance $L_s$ on the power losses and the switching behavior. Furthermore, measures to reduce overvoltage when using standard half-bridge modules to build a NPC 3-level topology are presented.
2. Device Under Test and Test Setup

As shown in Figure 2, the device under test is a 600A/1200V rated power module SEMiX603GB12E4p [2] that belongs to the SEMiX3p product family. It is a standard half-bridge module consisting of a TOP and BOT IGBT/Diode. It uses IGBT E4 and Diode CAL4F technology. For the test setup 12 capacitors (type: EPCOS 420uF B2520-B1227-A101) are connected in parallel that form together with the laminated busbar the DC-Link. The power module is mounted on a heatsink and screwed to the DC-Link. The DC-Link inductance $L_s$ is increased by increasing the distance between the DC-Link and the power module. This Application Note examines the switching behavior and losses for the following DC-Link inductances: $L_s=35/60/85\,\text{nH}$

The investigations at very high DC-Link inductances ($L_s=85\,\text{nH}$) are mainly used to illustrate the challenges of overvoltage issues of 3-level topologies based on standard half-bridge modules.

The statements on DC-Link inductances can be transferred to other current ratings if the inductance per ampere is considered. Thus, a 60nH inductance for a 600A rated module would be comparable to 120nH inductance for a 300A rated module.
3. Influence of \( L_s \) on switching performance and power losses

3.1 Overview

Figure 3 shows the quantities whose dependence on \( L_s \) is discussed in this Application Note.

**Figure 3: Investigated quantities that depend on DC-Link inductance \( L_s \)**

- Power Losses
- Overvoltage
- Delay times
- Diode reverse recovery behaviour

3.2 Influence of \( L_s \) on Power losses

3.2.1 Influence of \( L_s \) on IGBT Turn-on losses \( E_{on} \)

Figure 4 shows the influence of \( L_s \) on the IGBT turn-on losses \( E_{on} \). With increasing inductance the voltage drop of the \( V_{dc} \) voltage increases. In this case one speaks of inductive voltage drop. Due to the constant DC-Link voltage, the \( \frac{di}{dt} \) decreases with increasing inductance, which is visible from the turn-on current \( I_c \). The multiplication of \( V_{dc} \) and \( I_c \) results in the turn-on losses \( E_{on} \) for the three DC-Link inductances. As the turn-on resistance \( R_{on} \) increases, the \( L_s \) caused difference in turn-on losses remains almost constant. Only towards low turn-on currents the differences decrease, because the inductive voltage drop disappears more and more. At 600V, 600A, 2\( \Omega \), 150°C the turn-on losses decrease by 25% in the range of \( L_s =35 \) to 85nH.

**Figure 4: Influence of \( L_s \) on IGBT Turn-on losses \( E_{on} \)**

- \( V_{dc} =600V \), \( I_c =600A \), \( R_{on} =2\Omega \), \( T_j =150°C \)
- \( L_s =35nH \)
- \( L_s =60nH \)
- \( L_s =85nH \)
3.2.2 Influence of $L_s$ on IGBT Turn-off losses $E_{\text{off}}$

Figure 5 shows the influence of $L_s$ on the IGBT turn-off losses $E_{\text{off}}$. With increasing inductance the overvoltage across the IGBT increases. Due to the increasing overvoltage and the decreasing $dV/dt$, the switching losses increase with increasing DC-Link inductance. With increasing turn-off resistance $R_{\text{off}}$ the difference in turn-off losses remains almost constant. Only towards small turn-off currents do the differences decrease. At 600V, 600A, $2\Omega$, 150°C the turn-off losses increase by 14% in the range of $L_s=35$ to 85nH.

![Figure 5: Influence of $L_s$ on IGBT Turn-off losses $E_{\text{off}}$](image)

| $V_{dc}$=600V, $I_s$=600A, $R_{\text{on/off}}=2\Omega$, $T_j=150^\circ$C | $L_s=35\text{nH}$ | $L_s=60\text{nH}$ | $L_s=85\text{nH}$ |

3.2.3 Influence of $L_s$ on IGBT total losses $E_{\text{sw}}$

Figure 6 shows $E_{\text{on}}$, $E_{\text{off}}$ and the sum of both $E_{\text{sw}}$ as relative values over the DC-Link inductance $L_s$. The total switching losses $E_{\text{sw}}$ refer to the reference value at $L_s=35\text{nH}$. $E_{\text{on}}$, $E_{\text{off}}$ refer to the respective total losses $E_{\text{sw}}$ at the corresponding DC-Link inductance. At 600V, 600A, $2\Omega$, 150°C, the total switching losses decrease by about 10% in the range of $L_s=35$ to 85nH.

![Figure 6: Influence of $L_s$ on IGBT total losses $E_{\text{sw}}$](image)
3.2.4 Influence of \( L_s \) on Diode Turn-off losses \( E_{rr} \)

Figure 7 shows the influence of \( L_s \) on the diode turn-off losses \( E_{rr} \). With increasing inductance the course of the voltage rise over the diode changes, the \( dI/dt \) decreases and the losses increase. With increasing turn-on resistance \( R_{gon} \) the difference in turn-off losses remains almost constant. Only towards small turn-off currents do the differences decrease. At 600V, 600A, 2\( \Omega \), 150°C the turn-off losses increase by 14% in the range of \( L_s = 35 \) to 85nH.

3.3 Influence of \( L_s \) on Overvoltage

3.3.1 Influence of \( L_s \) on IGBT overvoltage during Turn-off

Figure 8 shows the influence of \( L_s \) on IGBT overvoltage during turn-off. All curves are synchronized with each other at the gate-emitter voltage \( V_{ge} \). With increasing inductance the overvoltage and the oscillations increase. The oscillations are visible in the \( V_{ge} \), \( V_{ce} \), voltage and the switched current. The overvoltage as a function of \( R_{gon} \) shows a typical IGBT4 behavior. It first increases with increasing resistance and then decreases again. At 600V, 400A, 2\( \Omega \), 25°C the overvoltage related to \( V_{dc} \) doubles (528V overvoltage compared to 260V) in the range of \( L_s = 35 \) to 85nH.
3.3.2 Influence of $L_s$ on Diode overvoltage during Turn-off

Figure 9 shows the influence of $L_s$ on Diode overvoltage during turn-off. All curves are synchronized with each other at the gate-emitter voltage $V_{ge}$. With increasing inductance the overvoltage and the oscillations increase. The oscillations are visible in the $V_{pg}, V_{ph}$ voltage and the switched current. The overvoltage as a function of $R_{gon}$ shows that from a gate resistance of 4 or $6\Omega$ no overvoltage occurs anymore. However, this is accompanied by an increase in the IGBT turn-on losses $E_{gon}$ (refer to Figure 4). At 600V, 25A, $2\Omega$, 25°C the overvoltage related to $V_{dc}$ quadruples in the range of $L_s$=35 to 85nH.

![Figure 9: Influence of $L_s$ on Diode overvoltage during Turn-off](image)

3.4 Influence of $L_s$ on delay times

3.4.1 Influence of $L_s$ on Turn-on delay time $t_{d_{on}}$

Figure 10 shows the influence of $L_s$ on turn-on delay time $t_{d_{on}}$. All curves are synchronized with each other at the gate-emitter voltage $V_{ge}$. With increasing inductance the di/dt changes what causes the turn-on delay time only slightly to change. At 600V, 600A, $2\Omega$, 150°C the influence on the turn-on delay time can be neglected in the range of $L_s$=35 to 85nH.

![Figure 10: Influence of $L_s$ on Turn-on delay time $t_{d_{on}}$](image)
3.4.2 Influence of $L_s$ on Turn-off delay time $t_{d\_off}$

Figure 11 shows the influence of $L_s$ on turn-off delay time $t_{d\_off}$. All curves are synchronized with each other at the gate-emitter voltage $V_{ge}$. With increasing inductance the $di/dt$ changes what causes the turn-off delay time on slightly to change. At 600V, 600A, 2$\Omega$, 150°C the influence on the turn-on delay time can be neglected in the range of $L_s=35$ to 85nH.

![Figure 11: Influence of $L_s$ on Turn-off delay time $t_{d\_off}$](image)

$V_{dc}=600V$, $I_s=600A$, $R_{gon}=2\Omega$, $T_j=150°C$  
$L_s=35nH$  
$L_s=60nH$  
$L_s=85nH$

3.5 Influence of $L_s$ on Diode Reverse Recovery behavior

3.5.1 Influence of $L_s$ on maximum reverse recovery peak current $I_{rrm}$

Figure 12 shows the influence of $L_s$ on the maximum reverse recovery peak current $I_{rrm}$. All curves are synchronized with each other at the gate-emitter voltage $V_{ge}$. With increasing inductance the $I_{rrm}$ changes only slightly. The differences in $I_{rrm}$ keep constant also at higher $R_{gon}$.

![Figure 12: Influence of $L_s$ on maximum reverse recovery peak current $I_{rrm}$](image)

$V_{dc}=600V$, $I_s=600A$, $R_{gon}=2\Omega$, $T_j=150°C$  
$L_s=35nH$  
$L_s=60nH$  
$L_s=85nH$
4. 3-Level Topologies based on Standard half-bridge modules

4.1 NPC topology based on SEMIX3p

3-level topologies are state of the art and are used in grid tie inverters mainly in wind, solar and UPS applications. In Figure 13 a Neutral Point Clamp (NPC) topology is shown, which is constructed from three standard half-bridge modules. Due to the terminal connections for DC+/DC-/N and AC, the DC-Link cannot be designed in such a way that the potentials overlap completely. This leads to an increased DC-Link inductance, which differs significantly from that specified in the data sheet of the module.

Figure 13: NPC topology based on standard half-bridge modules

4.2 Commutation loops

4.2.1 Commutation loops at power factor = 1

The commutation loops over an output period are shown for the power factor = 1 in Figure 14. The phase angle between the idealized output voltage and current is 0°. For positive and negative output current, fast commutation takes place exclusively within a half-bridge module. The commutation inductance is of the same order of magnitude as that specified in the module data sheet. From the point of view of overvoltage limitation, the voltage zero crossing must be considered here when fast commutation changes from DC+/N to N/DC- or vice versa. In this commutation case all three modules are involved. Due to the single switching event within an output period, the gate resistances for T2/T3 can be chosen large, however, so that the switching losses can be neglected.

Figure 14: Commutation loops at power factor = 1
4.2.2 Commutation loops at power factor = -1

The commutation loops over an output period are shown for the power factor = -1 in Figure 15. The phase angle between the idealized output voltage and current is 180°. For positive and negative output current, all three half-bridge modules are always involved in the fast commutation. The commutation inductance is much higher than the values given in the data sheet and can reach values of 100nH or even more.

Figure 15: Commutation loops at power factor = -1

Figure 16 shows the overvoltage curves to be expected when switching off the IGBT T2/T3 and the diodes D1/D4 as a function of the commutation inductance (see Figure 8/Figure 9). For the IGBT, the overvoltage increases with falling temperature and rising turn-off currents. In this example, an overvoltage of 1128V at 400A/Lc=85nH occurs at the IGBT. For the diode, low currents and high temperatures are critical. Here an overvoltage of 1106V at 25A/Lc=85nH occurs. In both cases the maximum overvoltage of approx. 70V or 90V is only slightly below the maximum permissible blocking voltage of 1200V.

Figure 16: Overvoltage at T2/T3 and D1/D4

Vdc=600V, Rgoff=2Ω, IGBT: Ic=400A, Tj=25°C; Diode: Id=25A, Tj=150°C  Lc=35nH  Lg=60nH  Lg=85nH

Figure 17 shows the overvoltage characteristics of the IGBT and diode as a function of the gate resistance. The characteristic of Lc=100nH is estimated and symbolized by a dotted line. Corresponding to the maximum turn-off current, the Rgoff must be increased for a given DC-Link design to remain below the maximum blocking voltage. In this example, the IGBT overvoltage exceeds the maximum blocking voltage of 1200V at an inductance of 100nH. To achieve the same 860V overvoltage at Lc=100nH as at 35nH would require to increase Rgoff from 2Ω to well more than 100, if it is achieved at all. With increasing Rgoff the losses increase (see Figure 5).
It can be seen from Figure 9 that the maximum overvoltage of the diode occurs at approx. 25A, which is in the range of 5% of the nominal chip current. This current value always occurs near the current zero crossing regardless of the maximum output power. To generate the same overvoltage at the diode at $L_s=100\text{nH}$ as at $35\text{nH}$, the $R_{gon}$ would have to be increased from 2 to $5.5\Omega$. Referring to Figure 4, the turn-on losses are almost doubled if the $R_{gon}$ is increased from 2 to $5.5\Omega$.

**Figure 17: Overvoltage at T2/T3 and D1/D4**

<table>
<thead>
<tr>
<th>$V_{dc}=600V$, IGBT: $I_c=400A$, $T_j=25\text{°C}$; Diode: $I_F=25A$, $T_j=150\text{°C}$</th>
<th>$L_s=35\text{nH}$</th>
<th>$L_s=60\text{nH}$</th>
<th>$L_s=85\text{nH}$</th>
<th>$L_s=100\text{nH}$ (estimated)</th>
</tr>
</thead>
</table>

**5. Summary**

In this Application Note, the influence of the DC-Link inductance on the switching behavior and the power losses was examined. It was shown that with increasing DC-Link inductance $L_s$, the IGBT turn-on losses decrease, whereas IGBT and diode turn-off losses increase. $E_{on}$ in particular is reduced more than $E_{off}$ and $E_{rr}$ increase. This is the reason why $L_s$ is given in the data sheet, otherwise the losses can be assumed too optimistically.

Furthermore, the overvoltage and the tendency to oscillate increase with increasing inductance for both the IGBT and the diode. This makes it necessary to increase the gate resistance with increasing stray inductance, which leads to higher losses.

The influence on the turn-on and turn-off delay time can be neglected.

Even though increased DC-Link inductance results in reduced $E_{on}$, a low-inductance DC-Link design should still be aimed for, since low overvoltage peaks are essential for reliable operation. In addition, a low-inductance DC-Link design is necessary in order to turn-off high output currents even in the event of a short circuit and to limit the overvoltage and oscillations on the IGBT and the diode during turn-off (EMI).

In the case of 3-level NPC topologies based on standard half-bridge modules, other gate resistances than those specified in the data sheet must be used, as in this case the commutation inductance can be much higher than that specified in the data sheet.

Furthermore, when comparing power dissipation in different data sheets, it is important to note at which inductance they were measured.
## Symbols and Terms

<table>
<thead>
<tr>
<th>Letter Symbol</th>
<th>Term</th>
</tr>
</thead>
<tbody>
<tr>
<td>AC</td>
<td>Output terminal</td>
</tr>
<tr>
<td>DC+</td>
<td>Positive potential (terminal) of a direct voltage source</td>
</tr>
<tr>
<td>DC-</td>
<td>Negative potential (terminal) of a direct voltage source</td>
</tr>
<tr>
<td>di/dt</td>
<td>change of current per time</td>
</tr>
<tr>
<td>DUT</td>
<td>Device Under Test</td>
</tr>
<tr>
<td>dv/dt</td>
<td>change of voltage per time</td>
</tr>
<tr>
<td>E_{off}</td>
<td>Energy dissipation during IGBT turn-off time</td>
</tr>
<tr>
<td>E_{on}</td>
<td>Energy dissipation during IGBT turn-on time</td>
</tr>
<tr>
<td>E_{rr}</td>
<td>Energy dissipation during reverse recovery (diode)</td>
</tr>
<tr>
<td>E_{sw}</td>
<td>Energy dissipation during IGBT turn-off and turn-on time</td>
</tr>
<tr>
<td>I_c</td>
<td>Continuous collector current</td>
</tr>
<tr>
<td>I_f</td>
<td>Diode forward current</td>
</tr>
<tr>
<td>IGBT</td>
<td>Insulated Gate Bipolar Transistor</td>
</tr>
<tr>
<td>I_{nom}</td>
<td>Nominal current</td>
</tr>
<tr>
<td>I_{rrm}</td>
<td>Peak reverse recovery current</td>
</tr>
<tr>
<td>L_{CE}</td>
<td>Parasitic collector-emitter inductance</td>
</tr>
<tr>
<td>L_s</td>
<td>DC-Link stray inductance</td>
</tr>
<tr>
<td>N</td>
<td>Neutral potential (terminal) of a direct voltage source; midpoint between DC+ and DC</td>
</tr>
<tr>
<td>R_{gon}</td>
<td>Gate turn-on resistor</td>
</tr>
<tr>
<td>R_{goff}</td>
<td>Gate turn-off resistor</td>
</tr>
<tr>
<td>t</td>
<td>Time</td>
</tr>
<tr>
<td>t_{d_off}</td>
<td>Turn-off delay time</td>
</tr>
<tr>
<td>t_{d_on}</td>
<td>Turn-on delay time</td>
</tr>
<tr>
<td>t_f</td>
<td>Fall time</td>
</tr>
<tr>
<td>t_r</td>
<td>Rise time</td>
</tr>
<tr>
<td>V_{ce}</td>
<td>Collector-emitter voltage</td>
</tr>
<tr>
<td>V_{ces}</td>
<td>Collector-emitter voltage with gate-emitter short circuited</td>
</tr>
<tr>
<td>V_{dc}</td>
<td>Total supply voltage (DC+ to DC-)</td>
</tr>
<tr>
<td>V_{FWD}</td>
<td>Voltage across free-wheeling diode</td>
</tr>
<tr>
<td>V_{ge}</td>
<td>Gate-Emitter voltage</td>
</tr>
<tr>
<td>V_{RRM}</td>
<td>Repetitive peak reverse voltage (Diode)</td>
</tr>
<tr>
<td>T_j</td>
<td>Junction temperature</td>
</tr>
<tr>
<td>\omega t</td>
<td>Conduction angle</td>
</tr>
</tbody>
</table>

A detailed explanation of the terms and symbols can be found in the “Application Manual Power Semiconductors” [3]

## References

[1] www.SEMIKRON.com
[2] SEMiX603GB12E4p, data sheet, Rev. 2.0 – 25.01.2017
IMPORTANT INFORMATION AND WARNINGS

The information in this document may not be considered as guarantee or assurance of product characteristics ("Beschaffenheitsgarantie"). This document describes only the usual characteristics of products to be expected in typical applications, which may still vary depending on the specific application. Therefore, products must be tested for the respective application in advance. Application adjustments may be necessary. The user of SEMIKRON products is responsible for the safety of their applications embedding SEMIKRON products and must take adequate safety measures to prevent the applications from causing a physical injury, fire or other problem if any of SEMIKRON products become faulty. The user is responsible to make sure that the application design is compliant with all applicable laws, regulations, norms and standards. Except as otherwise explicitly approved by SEMIKRON in a written document signed by authorized representatives of SEMIKRON, SEMIKRON products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury. No representation or warranty is given and no liability is assumed with respect to the accuracy, completeness and/or use of any information herein, including without limitation, warranties of non-infringement of intellectual property rights of any third party. SEMIKRON does not assume any liability arising out of the applications or use of any product; neither does it convey any license under its patent rights, copyrights, trade secrets or other intellectual property rights, nor the rights of others. SEMIKRON makes no representation or warranty of non-infringement or alleged non-infringement of intellectual property rights of any third party which may arise from applications. This document supersedes and replaces all information previously supplied and may be superseded by updates. SEMIKRON reserves the right to make changes.

SEMIKRON INTERNATIONAL GmbH
Sigmundstrasse 200, 90431 Nuremberg, Germany
Tel: +49 911 6559 6663, Fax: +49 911 6559 262
sales@semikron.com, www.semikron.com